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PLANAR INTEGRATION OF THIN FILM UNITS

Report Nr. 4

Department of the Army Contract Nr. DA-36-039 AMC-03732(E)

Department of the Army Project Nr. 1P6-22001-A-057.(3A99-15-005)

Final Report

15 January 1964 to 14 January 1965

U.S. ARMY ELECTRONICS LABORATORIES
Fort Monmouth, New Jersey

WESTINGHOUSE DEFENSE AND SPACE CENTER
AEROSPACE DIVISION
BALTIMORE, MARYLAND

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Signal Corps Technical Requirement Nr. SCL-7638B

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FINAL REPORT

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The object of this study is to establish and demonstrate highly reliable and practical methods for mounting and subsequent simultaneous interconnection of discrete "chip" parts and silicon semiconductor integrated circuits to previously deposited thin film circuitry on a common micro-circuit wafer.

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1. PURPOSE

The purpose of this contract is the advancement of a practical microminiature system for compliant planar electrical interconnections between thin film circuits, discrete parts and solid circuits. The advanced types of discrete parts and circuits of interest are those which are in the microminiature "chip" and silicon semiconductor integrated circuit form which are suitable for recessing flush with one surface of a microcircuit wafer. It is a design objective that the deposited interconnection shall have a mean-time-to-failure to 10^9 hours at a 60 percent confidence level.

1.1 OBJECTIVES

The overall assembly and process system shall provide deposited conductors which are adequately compliant to ensure reliable interconnections across the dissimilar materials between terminations on the "chip" parts and silicon semiconductor integrated circuits, and the corresponding terminations on the microcircuit wafer. The overall assembly and process system is intended to utilize inorganic microwafers containing suitable "blind recesses" for mounting the "chip" parts and silicon semiconductor integrated circuits of interest. After fastening in position, the surfaces of the "chip" parts and silicon semiconductor integrated circuits shall be essentially flush with the surface of the microwafer. Materials and processes shall provide a suitable surface between the terminal areas on the microwafer surface and the corresponding terminal areas on the "chip" part or silicon semiconductor integrated circuit to permit subsequent formation of an interconnecting conductor having the requisite compliance. Interconnections shall then be deposited to provide a reliable compliant conducting path across the dissimilar materials and disparate levels existing between the terminal areas of the "chip" parts, silicon semiconductor integrated circuits, and thin film circuitry. The deposited connections shall be suitable for use on microcircuit wafers which will be assembled into micro-circuit modules. Internal operating temperatures of micro-circuit modules will be 125°C. Desired projected capability is 200°C. The assembly and process system shall be evaluated by means of appropriate models, tested in accordance with specification SCL-7638B, "Planar Integration

of Thin Film Units".

1.2 TASK BREAKDOWN

Task A

This task provides for the development and demonstration of high reliability deposited interconnections between terminations on "chip" and silicon semiconductor integrated circuits and thin film terminations on glass and alumina microcircuit wafers. The objective of this task is to develop and demonstrate a deposited connection which will reliably bridge the dissimilar materials and disparate levels of the "chip" parts, silicon semiconductor integrated circuits, supporting materials and microwafers without degrading the resistance of the interconnection.

Task B

This task provides for the establishment of assembly fixtures and masking techniques for the assembly and interconnection of "chip" and silicon semiconductor integrated circuits with thin film network having stringent dimensional and orientation characteristics. Materials and techniques developed under Task A will be utilized under this task.

1.3 RELATED PROGRAMS

Work is being done for the Navy under contract NObsr 81380 on development of a molecularized pulse amplifier packaged with vapor deposited interconnections by techniques similar to those employed in this study. In addition, the Molecular Systems Section is engaged a study of vapor deposition of interconnections over dissimilar surfaces as part of a Westinghouse independent research and development program. A number of programs on thin film techniques are continually progressing within the Baltimore Defense and Space Center. Among these there are programs of fabrication of thin film passive networks for use in an ultra reliable transceiver under contract NONR-4189(00) and a frequency and time control system under contract NObsr-87593. Work being done on semiconductor devices

under several contracts makes extensive use of several thin film interconnection techniques.

2. ABSTRACT

2.1 BRIDGING MATERIAL PROCESS DEVELOPMENT

Three organic materials and five inorganic materials were investigated. On the basis of a preliminary thermal cycle test run with a square chip, Zerifac filled Doryl was selected as the candidate bridging material to be used for the experimental models. A cure cycle ending at 200°C for 2 hours was used. Examination under polarized light showed only slight strains, comparable to those observed in 150°C cured alumina-filled Doryl.

The resin was screened through a 124-mesh silk for the experimental models.

The stress analysis study indicated that the theoretical guidelines would not be met by the preselected materials and geometry, therefore non-linear properties in the bridging material would be needed to make up for the thermal expansion mismatch.

2.2 SUBSTRATE AND DUMMY COMPONENT FABRICATION

The substrates were perforated with an ultrasonic impact grinder. Chips were cut from scrap silicon wafers and Corning 0211 glass using hollow tubes for drills, once again using impact grinding. A special jig was used to hold and register substrates for drilling. Four patterns were drilled at a time in a 2 x 2" substrate.

2.3 THIN FILM DEPOSITION TECHNIQUE

A microcircuit jig installed in the vacuum system was used for deposition of metal film conductors and pads. Due to the curing temperatures required by the resin, copper and aluminum films were found to be adversely affected during the model fabrication. Techniques were developed to overcome this situation. Chromium was used in all cases as a bonding film to improve adhesion. For the interconnects the bulk of the film was made of copper followed by a gold flash for prevention of oxidation of the copper. The

interconnects, were approximately 0.0004 inch thick.

2.4 TEST AND EVALUATION

All samples passed adhesion tests with the exception of reworked aluminum pads on glass. In this case, poor adhesion was found between the oxidized aluminum and chrome-gold.

The low temperature storage models failed to meet specified objectives although no catastrophic failures were noted.

The moisture resistance test showed excellent leakage resistance although three out of ten specimens did not meet objective of ten megohms resistance at conclusion of test. Silastic 140 was used as a protective covering. The models failed to pass thermal shock test with 24 samples failing catastrophically.

A lower incidence of cracking was noted for the Doryl in the glass substrate. A failure mechanism study was conducted on the relative adhesiveness of Doryl to the glass and alumina. The glass was found to have a lower adhesion. Based on this observation it is believed that the Doryl in the glass substrates actually separated at the interface.

Mechanism of failure studies also showed that the prolonged exposure of Doryl to heat in vacuum was responsible for the failures observed.

3. PUBLICATIONS, LECTURES, REPORTS, AND CONFERENCES

3.1 PUBLICATIONS AND LECTURES

No publications or lectures during this program.

3.2 REPORTS

First Quarterly Progress Report on Planar Integration of Thin Film Units, Report No. 1, 15 January to 14 April 1964.

Second Quarterly Progress Report on Planar Integration of Thin Film Units, Report No. 2, 15 April 1964 to 14 July 1964.

Third Quarterly Progress Report on Planar Integration of Thin Film Units, Report No. 3, 15 July 1964 to 14 October 1964.

3.3 CONFERENCES

Following is a list of conferences held during this program.

3.3.1 8 January 1964

A conference was held at Fort Monmouth, New Jersey on 8 January 1964. Personnel in attendance representing U.S. Army Electronics Laboratories were Messrs. Gerhold, Bassler and Geisler. Representatives for Westinghouse were Messrs. Gray, Winter, and Lauriente. Subjects discussed were overall objectives of contract, environmental test program, administrative details, scheduling, model delivery and reports.

3.3.2 6 March 1964

A conference was held at the Aerospace Division of Westinghouse, Baltimore, Maryland on 6 March 1964. Personnel in attendance representing U.S. Army Electronics Laboratories were Messrs. Bassler and Geisler. Representatives for Westinghouse were Messrs. Gray, Harper, Lauriente, and Winter. Subject discussed was progress on bridging material process development.

3.3.3 22 April 1964

A conference was held at Fort Monmouth, New Jersey on 22 April 1964. Personnel in attendance representing U.S. Army Electronics Laboratories were Messrs. Bassler and Geisler. Representatives for Westinghouse were Messrs. Lauriente and Winter. Subject discussed was bridging material process development. Agreement was reached that epoxy be dropped from list of candidate bridging materials and continue on with diphenyl oxide resin and glass.

3.3.4 28 May 1964

A conference was held at Fort Monmouth, New Jersey on 18 May 1964. Personnel in attendance representing U.S. Army Electronics Laboratories were Messrs. Bassler and Geisler. Representatives for Westinghouse were Messrs. Ernst, Lauriente, Staley, and Winter. The purpose of this meeting was to review techniques for mounting of square chips in square holes and use of Zerifac filler to reduce thermal expansion of diphenyl oxide resin.

3.3.5 10 July 1964

A conference was held at the Aerospace Division of Westinghouse Electric Corporation, Baltimore, Maryland on 10 July 1964. Personnel in attendance representing U.S. Army Electronics Laboratories were Messrs. Bassler and Geisler. Representatives for Westinghouse were Messrs. Ernst, Gray, Gregory, Harper, Lauriente, Staley, and Winter. Subjects discussed were financial expenditures, and progress on model fabrication. A tour of facilities was made.

3.3.6 22 September 1964

A conference was held at Fort Monmouth, New Jersey on 22 September 1964. Personnel in attendance representing U.S. Army Electronics Laboratories were Messrs. Bassler and Geisler. Representatives for

Westinghouse were Messrs. Lauriente and Winter. Subject discussed was best method for reworking of oxidized pads for low temperature tests. A tentative decision was made to etch the oxide off the copper pads and evaporate gold over the aluminum pads. A typical substrate containing eight models was examined.

3.3.7 23 October 1964

A conference was held at the Aerospace Division of Westinghouse Electric Corporation, Baltimore, Maryland on 23 October 1964. In attendance representing U.S. Army Electronics Laboratories was Mr. Geisler. Representatives for Westinghouse were Messrs. Lauriente and Winter. The purpose of this meeting was to observe the techniques for evaporating the thin film circuits and discuss the thermal and humidity test samples.

3.3.8 25 November 1964

A conference was held at Fort Monmouth, New Jersey on 25 November 1964. Personnel in attendance representing U.S. Army Electronics Laboratories were Messrs. Bassler and Geisler. Representatives for Westinghouse were Messrs. Ernst, Lauriente and Winter. A discussion was held on the test data and results.

3.3.9 8 January 1965

A conference was held at Fort Monmouth, New Jersey on 8 January 1965. Personnel in attendance representing U.S. Army Electronics Laboratories were Messrs. Bassler and Geisler. Representatives for Westinghouse were Messrs. Lauriente and Winter. The final report was discussed.

4. FACTUAL DATA

4.1 DEVELOPMENT OF INTERCONNECTION TECHNIQUE (TASK A)

Development of a practical microminiature system for compliant planar electrical interconnections between thin film circuits, discrete parts and solid circuits requires a bridging material meeting the following properties:

a. It must be capable of physically supporting the chip inserts.
b. It must provide a surface compatible with vacuum deposited thin films, and be free from voids, cracks or other abrupt surface imperfections which would induce stresses.
c. It must have a thermal expansion compatible with the chip insert and substrate or have some other mechanical compensating property such as flexibility or ductility so as not to induce stresses to the overall system.

In addition to the above physical requirements, a practical technique is required for applying the material into the small spaces available and meeting other specifications of topology.

4.1.1 Analysis of the Problem

As a guide for achieving the objective a simple analysis was made of the stresses induced in the bridging material and deposited interconnection from thermal cycling. In these calculations, assumptions were made that all expansions remained in the elastic region, shear stresses parallel to boundaries were equal to zero, chip was centered in its hole, and coefficients of linear expansion were independent of temperature. Parameters were established as shown in Figure 4-1 where:

R_o = radius of hole in substrate at room temperature
r_o = radius of component at room temperature
D = depth of hole in substrate
α_c = linear thermal coefficient of expansion of component
α_s = linear thermal coefficient of expansion of substrate

α_f = linear thermal coefficient of expansion of bridging material.

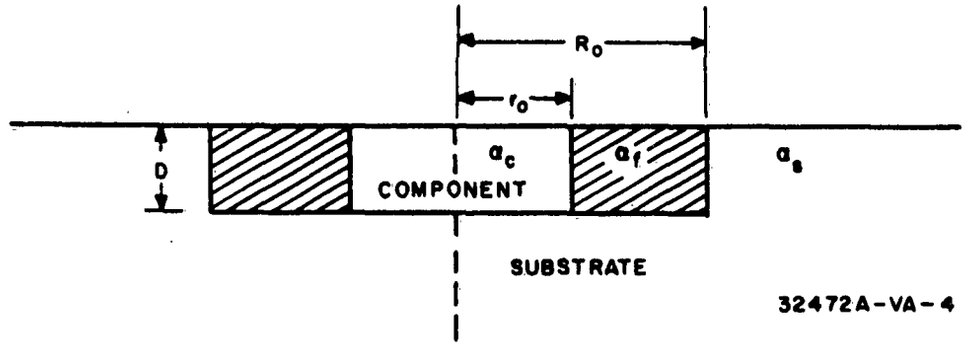

Figure 4-1. Diagram of Chip in Substrate Hole

With the approximation $3\alpha_f \cong \beta$, where β is the volume coefficient of thermal expansion of the filler material, an expression was derived

$$R_o/r_o^{\,2} = \frac{\beta - 2\alpha_c - \alpha_s}{\beta - 3\alpha_s} \qquad (1)$$

which is a statement that the changes with temperature of the volume of bridging material exactly match the volume change of the gap between chip and substrate. Solutions for the non-trivial cases were given by hyperbolas with asymptotes at $R_o/r_o = 1$ and $\alpha_f/\alpha_s = 1$. Curves representative of one family of solutions to equation (1) are shown in Figure 4-2. Only solutions with a physical meaning were considered. With $R_o/r_o \geq 1$, values of $\alpha_f > \alpha_s$ when $\alpha_c/\alpha_s < 1$ and $\alpha_f < \alpha_s$ where $\alpha_c/\alpha_s > 1$ were obtained. Solutions in the region $\alpha_c/\alpha_s > 1$ were discarded, because, inorganic materials with $\alpha_f < \alpha_s$ have too high a melting point to be of practical use. As borne out in data in Tables 4-1 and 4-2 of typical low temperature glasses and chip/substrates respectively, α_s is typically 32.5 - 64 x $10^{-7}/C^o$ whereas solder glasses less than 89 x $10^{-7}/C^o$ cure above 500°C. The first guideline therefore states that thermal expansion of substrate should be

Table 4-1

Solder Glass Information Data*

Solder** Glass Number	Type	Cuv. Temp. for 1 Hr.	Thermal Expansion x $10^{-7}/^{\circ}C$
SG-7	Vitreous	590°C	46 (0-300°C)
SG-67	Vitreous	430°C	82 (0-300°C)
SG-68	Vitreous	430°C	90 (0-300°C)
CV-97	Devit	440°C	93.5 (0-300°C)
CV-101	Devit	425°C	92 (0-300°C)
CV-130	Devit	425°C	107 (0-300°C)
CV-137	Devit	435°C	97 (0-300°C)
CV-285	Devit	625°C	55 (0-300°C)
CV-635	Devit	685°C	56 (0-300°C)

*K. G. Lusher, Proc. Ninth Symposium on the Art of Glassblowing (1964), The American Scientific Glassblowers Society, 309 Georgetown Avenue, Gwinhurst, Wilmington, Delaware 19803.

**Owens-Illinois Glass Company.

Table 4-2

Thermal Expansion of Chip and Substrate

Chip/Substrate	α_c/α_s $10^{-7}/^{\circ}C/10^{-7}/^{\circ}C$
0211/Al_2O_3	72/64
Si/Al_2O_3	28/64
0211/0211	72/72
0211/Si	72/28 (1)
0211/7740	72/32.5
Si/7740	28/32.5

7740, 0211 glass manufactured by Corning Glass Works, Corning, New York. Al_2O_3 supplied as AlSiMag 614, American Lava Corporation, Chattanooga, Tennessee.

(1) L. Maissel, Thermal Expansion of Silicon, J.A.P., 31, 211, Jan. 1960.

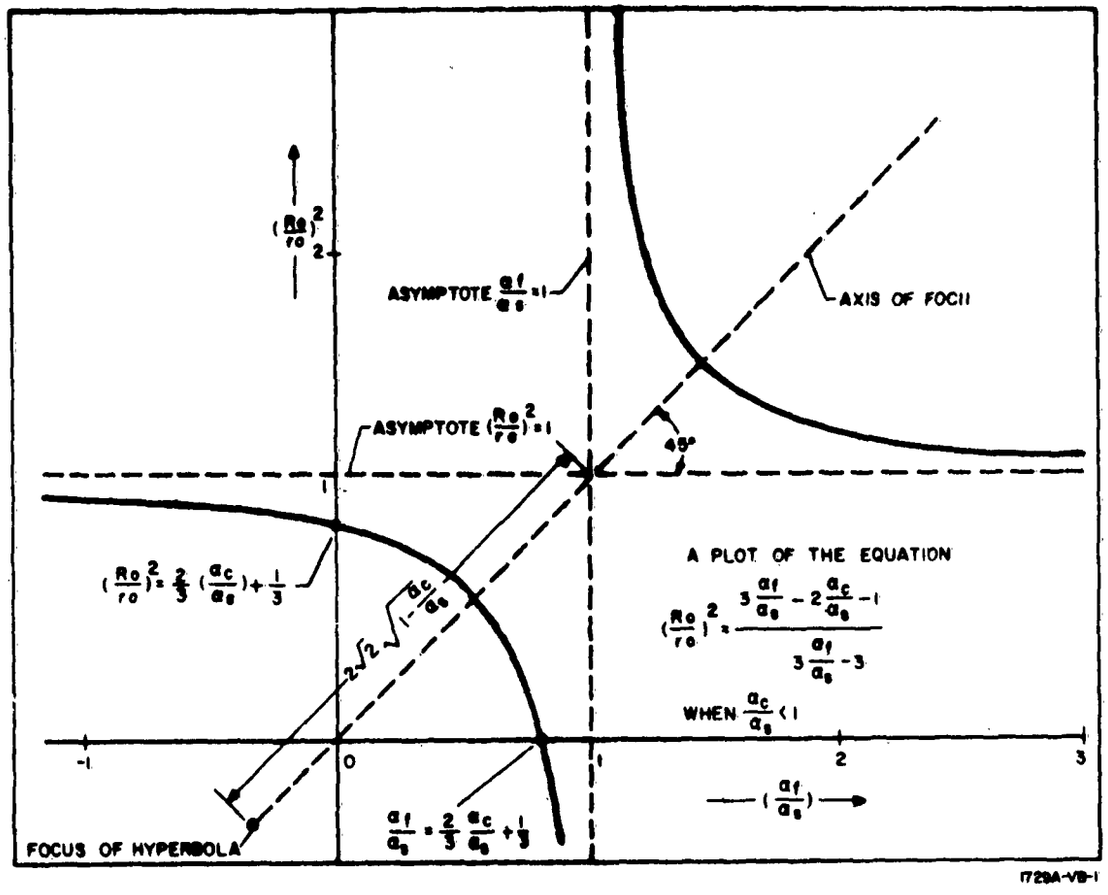

Figure 4-2. Ratio of Radii Versus Filler Expansion Coefficient $\alpha_c < \alpha_s$

greater than that of the chip.

From the equation*

$$S_{MAX} \cong -E\left\{\frac{18D^2\,\delta^2\,(T_d - T_o)^2}{(R_o - r_o)^2} + \frac{(T_d - T_o)\,(R_o\alpha_s - r_o\alpha_s)}{R_o - r_o} - (T_d - T_o)\,\alpha_{cond}\right. \quad (2)$$

where E = Young's modulus for the conductor

T = temperature

*"Planar Integration of Parts and Solid Circuits into Thin Film Units", Signal Corps Contract No. DA-36-039 SC-89109, 1st Quarterly Report, Melpar, Inc., 31 July 1962, ASTIA AD-288803.

δ = the difference between the desired volume expansion of the bridging material and the actual expansion. The desired volume expansion is that given by equation (1).

o,d = subscripts referring to room temperature and temperature of conductor deposition respectively.

A calculation may be made of the stress in interconnecting films. Inserting reasonable values for each parameter shows the first term dominates. The objective, of course, is to reduce S_{MAX}. One such approach is to minimize the first term by making δ small. This leads us to the second guideline: To choose a bridging material to match as closely as possible the volume change of the hole.

As an alternate, the first term may also be reduced by minimizing $D/(R_o - r_o)$, which is the ratio of hole depth to gap between substrate and chip. This leads us to the third and last guideline which is to maximize the gap and minimize the depth of hole.

It was recognized that some aspects of these guidelines were not completely satisfied because of prior selection of materials and geometry. An inspection of Table 4-2 shows that the first guideline $\alpha_c/\alpha_s < 1$ is indeed violated in a number of cases. Calculations of α_f using equation (1) predicted the incompatibility of 7740 as a substrate. (Table 4-3)

In general the filler material will exert forces on the substrate and chip as well as the conductor, when the thermal expansion of the ideal filler is not exactly matched. These forces must be less than the magnitude which will fracture the chip, substrate, or filler. The magnitude of these forces depends on the magnitude of the mismatch in coefficient of thermal expansion.

It has been assumed that the filler material remains in the elastic region of deformation. If instead, it exhibits plastic flow, or ductility, to minimize the effect of its forces on the substrate and chip, regions of catastrophic failure may be prevented. There will still remain the problem of minimizing the stress in an interconnection deposited onto the plastically deforming filler, but in practice this stress can be reasonably low. So the conclusion was to either impose extremely stringent conditions on the allowed magnitude of mismatch of expansion coefficients, or to use a

class of materials which was capable of exhibiting plastic flow properties.

Table 4-3
Calculated α_f

Substrate	Chip	α_f (R_o/r_o = 1.4) x $10^{-7}/^oC$
7740	0211	5.5
7740	Si	36
Al_2O_3	0211	58
Al_2O_3	Si	89
0211	Si	103
0211	0211	72

4.1.2 Bridging Material Process Development

The original schedule called for a selection of the best candidate material as judged by results of preliminary tests. An assumption had been made on the basis of material characteristics that there would be need for little, if any development necessary. Test results however revealed that the best candidate material was only marginal for although the test was successful with the round chip, they were unsuccessful with the square chip. The schedule was modified to include more time for development of material. A change to a lower thermal expansion filler for the square chip. Figure 4-3 charts the process development.

A. Organic Bridging Material

Three organic materials were investigated initially: filled Doryl[1], filled epoxy[2] and glass resin[3].

1. Resiweld 7004 manufactured by H. B. Fuller Company, St. Paul, Minnesota.
2. Diphenyl Oxide varnish manufactured by Westinghouse Electric Corporation, Pittsburgh, Pa.
3. Glass Resin, Type 100 manufactured by Owens-Illinois Glass Company, Toledo, Ohio.

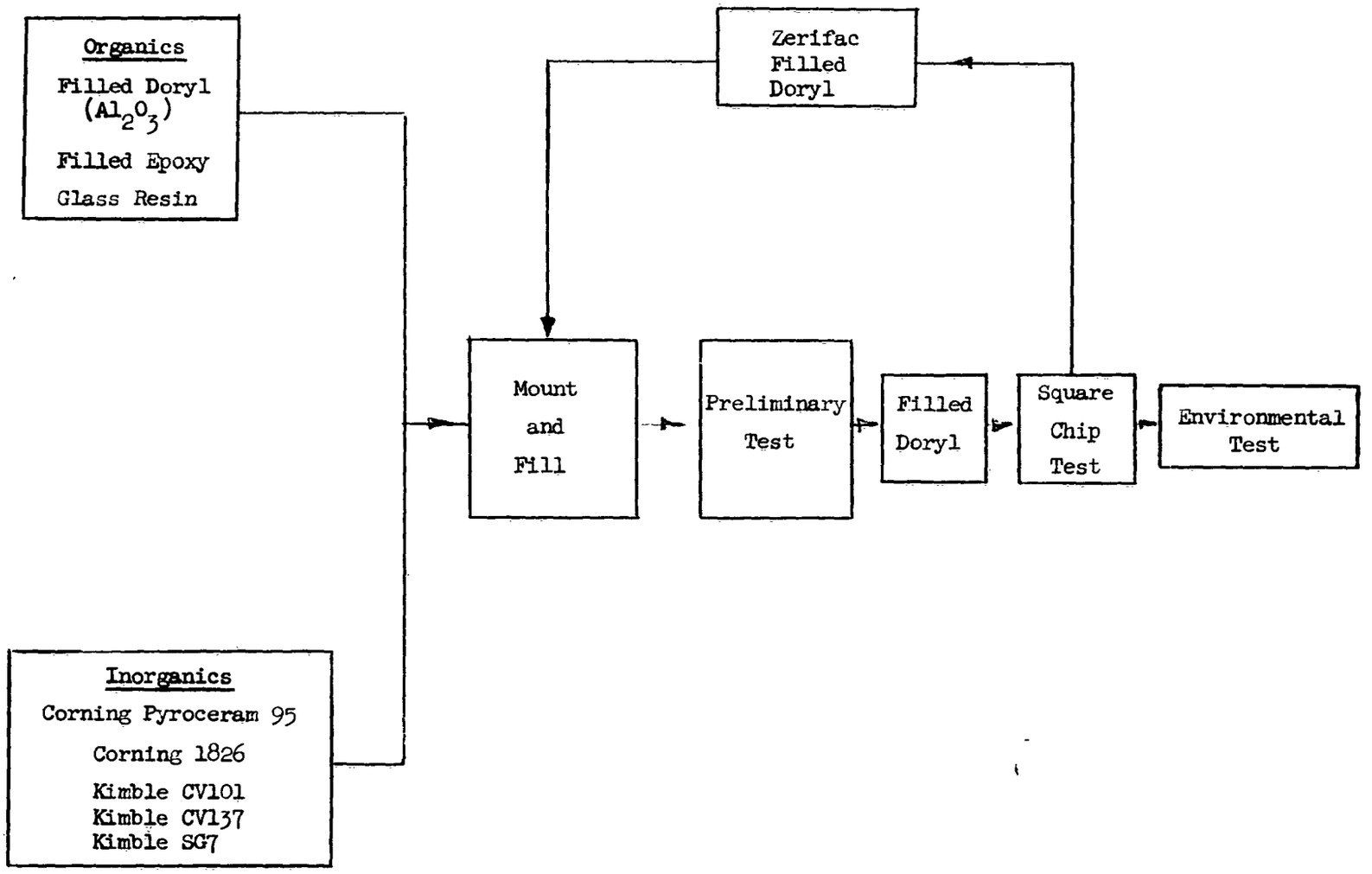

Figure 4-3. Chart of Bridging Material Process Development

1. Doryl

Properties of the varnish raw material and cured polymer are shown in Tables 4-4 and 4-5.

2. Resiweld 7004 Epoxy

This material was considered as a back-up for Doryl. Typical properties of Resiweld 7004 epoxy are given in Table 4-6. Figure 4-4 shows the rather significant effect that fillers have on the thermal expansion of epoxy.

3. Glass Resin

An investigation was also made of Owens-Illinois Glass Resin, Type 100.* This is a condensation polymer based on an alternating silicon-oxygen system so that they can be classed generically as silicones. Properties are given in Table 4-7. A screenable slurry was made up using 500 mesh aluminum oxide. The filled glass resin slides were dried at 50°C to form tack-free films and then cured for 24 hours at 90°C. Thermal shock tests (using acetone and dry ice) could not be conducted because of attack by acetone on the resin. Due to difficulties in applying the resin by screening techniques, no further work was done on this resin.

Table 4-4

Properties of Diphenyl Oxide Varnish

Solids	Supplied at 50 or 60 percent solids
Recommended Thinner	Toluol
Viscosity at 50 percent N.V.	30 - 80 sec. Demmler No. 1
Specific Gravity	1.010 - 1.020 at 50 percent solids 1.035 - 1.045 at 60 percent solids
Shelf Life	6 months
Cure Cycle (A) (B) (C)	2 Hrs. at 200°C 2 Hrs. at 250°C Longer periods at 150°C
Gel Time	5 - 10 minutes at 200°C (Can be regulated with addition of small amounts of inhibitors).

*Owens-Illinois Glass Resin General Bulletin NP-101

Table 4-5
Properties of Cured Diphenyl Oxide

BOND STRENGTH

Helical Coil Bond Strength (3 Mil Coating) - Cure A - 2 Hrs. at 200°C.
- Cure B - 2 Hrs. at 250°C.

At 25°C, Cure A or B	- 24 lb.
At 150°C, Cure B	- 22 lb.
At 150°C, after 300 Hrs. at 250°C	- 33 lb.
At 150°C, after 1000 Hrs. at 250°C	- 17 lb.
At 150°C, after 2000 Hrs. at 250°C	- 11 lb.

ELECTRICAL PROPERTIES

Dielectric Constant

	Frequency			
T°C.	60 Cycle	1 KC	100 KC	200 KC
25	3.91	3.89	3.82	2.81
100	3.89	3.85	3.81	--
150	3.86	3.81	3.75	3.75
200	4.36	4.11	3.84	3.83
250	5.83	5.32	4.50	4.40

Dissipation Factor

	Frequency			
T°C.	60 Cycle	1 KC	100 KC	200 KC
25	0.36	0.36	0.83	.90
100	0.51	0.46	0.45	--
150	0.56	0.59	0.63	.59
200	3.60	2.80	1.60	1.60
250	8.30	5.50	5.30	5.40

Dielectric Strength (ASTM) - Dry - 3000V/M - (Determined with 1/4" dia. sharp edged electrode under WEMCO "C" oil).

CHEMICAL RESISTANCE

(1) 16 hours at boiling points of materials listed below (run on aluminum panels):

Solvent	Vapor	Liquid
Toluol	No effect	Slight flaking and swelling
Ethyl Acetate	No effect	Slight cracking
Trichlorethylene	Slight flaking and swelling	Flaking and swelling
Methyl Ethyl Ketone	No effect	Slight cracking
Ethyl Alcohol	No effect	No effect

Resistance to Acids: Excellent

Resistance to Alkalies: Excellent

Table 4-6

Typical Properties of Resiweld 7004 Resin

Solids	100 percent
Base Resin	Epoxy
Viscosity at 25°C	Medium
Shelf Life	12 months
Cure Cycle	1 Hr. at 65°C
Gel Time	1 Hr. at 25°C

As Cured (1 hour at 65°C)

Tensile Shear Strength (Aluminum to Aluminum)

At 25°C	2000 psi
At 105°C	200 psi
At 150°C	125 psi

Hardness

"Shore D" Durometer at 25°C	75 - 85

Chemical Resistance

Resistance to most acids, bases, oil	Excellent
Resistance to most solvents	Excellent

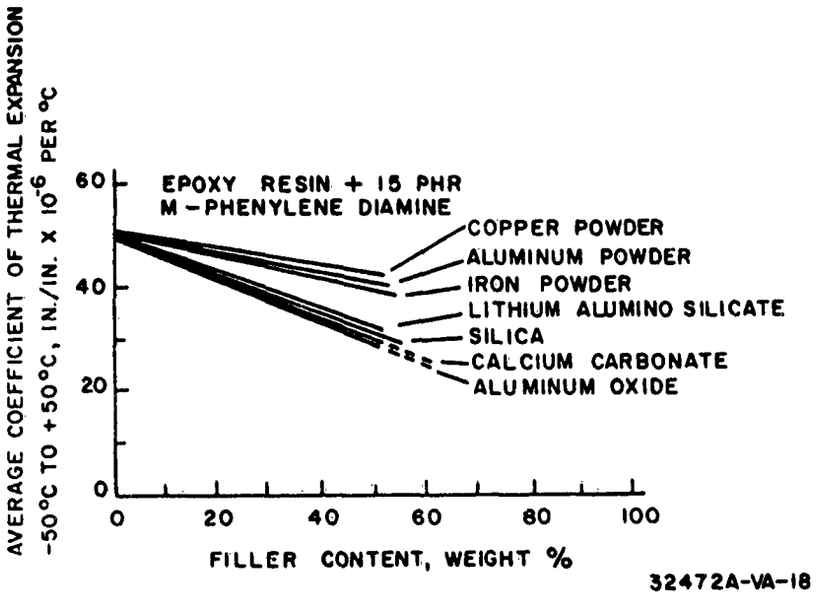

Figure 4-4. Effect of Various Fillers on Coefficient of Thermal Expansion of Epoxy Resin

B. Inorganic Bridging Material

The excellent chemical, electrical and thermal characteristics of glasses make them very attractive for the application called for in this study. A serious disadvantage of glasses, however, is the lack of ductility which places an especially stringent requirement for matching the thermal coefficient of expansion on any system where they are used. Because of the temperature limit of the component, only low temperature glasses were considered. These glasses fall into two general categories, devitrified and vitrified types.

1. Devitrified

The devitrified type might be compared to a thermosetting plastic since the glass after maturing has properties which enable it to be reheated at a reasonably high temperature without showing glassy flow. When first melted this type of glass is in a clear, vitreous state. On heating the glass begins to devitrify as evidenced by a gradual transformation to an opaque state. The temperature at which it is heated determines the type and size of crystals which will be formed in the devitrification.

This type and size of crystal in turn controls the thermal expansion of the product. When matured the product is stronger and harder than glass. Devitrified glasses evaluated were Corning Pyroceram 95,[1] and Kimble CV101 and CV137.[2] Properties given by the manufacturers are contained in Tables 4-6 and 4-9.

Table 4-7

Data O-I Glass Resin Type 100[3]

Electrical Properties

Dielectric Strength: (50 mil sample) Short Time (volts/mil) = 900

Volume Resistivity: (Ohm-cm) $25^{\circ}C = 1 \times 10^{14}/75^{\circ}C = 2 \times 10^{16}$

Dielectric Constant: 60 cycles = $4.1/10^{6}$ cycles = 3.2

Dissipation Factor: 60 cycles = $30 \times 10^{-4}/10^{6}$ cycles = 70×10^{-4}

Thermal Properties

Coefficient of Linear Expansion: $(0\text{-}300^{\circ}C) = 13 \times 10^{-5}/^{\circ}C$

Chemical Resistance

Solid, cured samples are non-flammable, chemically inert materials. They will not dissolve in organic solvents. The immersion of solid castings in acetone or alcohols for several hours at room temperature must be avoided, or surface crazing will result. Oxidizing and reducing agents do not affect Glass Resins except under extreme conditions. Concentrated solutions of alkali and hydrofluoric acids decompose the cured resins. Water absorption for a cured specimen two inches in diameter and one-eight thick at $23^{\circ}C$ for 24 hours results in an 0.8 percent weight increase.

Specifications

Solids Content: 60 percent Viscosity: $A_5\text{-}A_1$ Gel Temp: $180^{\circ}\text{-}200^{\circ}C$

1. Manufactured by Corning Glass Works, Corning, New York.
2. Manufactured by Kimble Glass Company, Toledo, Ohio.
3. Owens-Illinois General Bulletin NP-101

Table 4-8

PYROCERAM* CEMENT 95

GENERAL

The cement fires at a low temperature range of 400°C to 450°C depending on sealing time. This permits the joining of materials likely to deform at temperature much above 450°C. However, the crystalline seal is serviceable in use for temperatures up to 425°C.

PROPERTIES

Physical Properties

Young's Modulus	6.66×10^6 p.s.i.
Shear Modulus	2.62×10^6 p.s.i.
Poisson's Ratio	0.27
Modulus of Rupture at 25°C	6000.0 (approx.)
Modulus of Rupture at 425°C	15000.0 (approx.)
Density	6.5 (approx.)

Electrical Properties

Log DC Resistivity	at 250°C	8.550
	at 350°C	7.030

		100 Cycles	1 k.c.	100 k.c.
Loss Tangent	at 25°C	.0058	.0064	.0094
	at 230°C		.11	.0057
	at 373°C			.15
Dielectric Constant	at 25°C	21.2	21.0	20.4
	at 230°C		23.4	22.2
	at 373°C			25.2

Loss Factor = Loss Tangent x Dielectric Constant

*Corning trademark

Table 4-9

Properties of Solder Glass	CV-101*		CV-137*		SG-7**
Thermal Expansion 0-200°C	88×10^{-7}/°C		95×10^{-7}/°C		46×10^{-7}/°C
0-300°C	92×10^{-7}/°C		97×10^{-7}/°C		
0-425°C	94×10^{-7}/°C		101×10^{-7}/°C		
Note: Thermal expansion the devitrified solder glass depends on thermal history. These values are for curing cycles of one hour at 425°C-440°C.					
Thermal Contraction (annealing point to 25°C)					58×10^{-7}/°C
Viscosities					
Strain Point					456°C
Annealing Point					476°C
Softening Point					572°C
Density					4.08 gm/cc
Electrical Resistivity, ohm-cm, firing temperature:	410°C	440°C	410°C	440°C	
Log DC Resistivity at 25°C	12.6	12.4	12.2	10.2	
150°C	9.8	9.6	8.3	8.0	14.4
250°C	7.6	7.6	7.5	7.3	11.3
350°C	6.4	6.3	6.2	6.1	9.2
Dielectric Constant (ASTM D150-54T) one megacycle, K	19.3	17.4	18.2	17.9	8.16
Power Factor, one megacycle, Δ percent	1.2	1.8	1.7	--	0.16
Dielectric Strength (volts/mil DC at 0.050")	700		700		

*Devitrified
**Vitrified

2. Vitrified

The vitreous type is simple and low melting glass which can be applied to higher-melting glasses at temperatures below or just above their annealing points and effects a seal in the same way that metals are soldered. The properties of the two vitreous glasses evaluated, Kimble SG7 and Corning 1826, are given in Tables 4-9 and 4-10 respectively.

Table 4-10

Corning 1326 Solder Glass

GLASS CHARACTERISTICS

Expansion 0° to $300^{\circ}C$	49 x 10^{-7} in/in/$^{\circ}C$
Annealing Point	$454^{\circ}C$
Softening Point	$585^{\circ}C$
Strain Point	$430^{\circ}C$
Density	3.17 gms/cc
Log DC Resistivity at $250^{\circ}C$	10.0
Log DC Resistivity at $350^{\circ}C$	8.1

C. Mounting and Filling Technique for Preliminary Tests

A two-step filling process was employed by which an initial volume of filler material would be metered into the hole. For this phase, the mounting procedure was a hand operation. Only enough material was applied initially in the hole to retain the chip in place to withstand screening. The chip was then inserted manually. Because of the adaptability of all the materials to screening, there was no need to give consideration to an alternative technique for filling.

A facility was developed for making our own stencils. The stencils were made with Type 4570 Colograph* Presensitized Photostencil Film following the manufacturers directions.

*Supplied by McGraw Colograph Company, Burbank, California.

1. Doryl

Two approaches were initially considered, (1) making a solventless, small particle size diphenyl oxide powder which could be blended with suitable fillers and compounded with suitable dispersing agents for screening, and (2) making a highly filled, screenable formulation from the basic diphenyl oxide varnish, which could be slowly cured to remove the solvent. The first approach offered the advantages normally inherent in solvent free systems. However, early work on this approach indicated difficulty of developing a suitable screening formulation. Also, curing shrinkages resulting from removal of the dispersing agents during cure were such as to require multiple steps for complete filling of the gap between the chip and the substrate. Hence, efforts on this approach were abandoned.

In the second approach, the chip was bonded into the hole using a filled diphenyl oxide as the adhesive followed by screening of a thixotropic formulation. A two part formulation was developed consisting of the following ingredients, in parts by weight:

Part A	Part A	Part B
Diphenyl Oxide (B109-3)	100	100
Cab-O-Sil Thixotroping Agent*	6	2
Aluminum Oxide, 500 mesh	---	125

In these formulations, the viscosity of the base diphenyl oxide is controlled at 435 ± 5 cps at 25 ± 1°C (Brookfield Viscometer, No. 1 spindle at 20 RPM). Both formulations were ball milled for 24 hours to assure proper filler wetting and dispersion. This method of compounding also minimized air entrapment which occurs with many compounding methods.

Although one part formulations have been tried and used in this development program (i.e., combinations of Part A and Part B, it was found that by having two parts, and blending them as needed, a better control of the thixotropy-solvent balance transients resulted, especially for purposes of screening.

*Manufactured by Cabot Corporation, Boston, Massachusetts.

As was expected, much effort was also required to establish optimum resin curing which would both yield gradual trouble-free solvent release from the compound and provide a thorough cure which minimized stresses on the chip and substrate. The cure established was as follows: 2 hours at room temperature, followed by one hour each at 50°C, 65°C, 85°C, 100°C, 125°C, and 150°C. At 150°C, some strains developed in substrate, and at 175°C curing some fractures in chips developed.

2. Epoxy Resin Formulations

Two approaches were pursued: (1) using a small particle size epoxy powder which could be blended with suitable fillers and compounded with suitable dispersing agents for screening -- similar to the approach with powdered diphenyl oxide, and (2) making a highly filled, screenable formulation using a liquid epoxy resin, compounded with 500 mesh aluminum oxide and Cab-O-Sil thixotroping agent -- again similar to the diphenyl oxide liquid resin approach -- except that this epoxy formulation would have the advantage of being solvent free. Experiences with this first approach matched experiences with the powdered diphenyl oxide approach -- namely, screening and shrinkage problems, hence this approach was abandoned. The second approach, however, was successful, and an excellent screenable formulation resulted as follows, on a weight basis:

Resiweld Epoxy 7004	- 5 parts each of Part A and Part B
Aluminum Oxide, 500 mesh	- 17 parts
Cab-O-Sil Thixotroping Agent	- 0.1 part

Being solvent free, this screening formulation was evacuated for 5-10 minutes at 1-2 mm. Hg. The curing cycle was for two hours at room temperature followed by one hour each at 65°C, 100°C, 150°C. The absence of solvent allowed a more rapid cure than with diphenyl oxide. With this formulation, repetitively good screening resulted, and strains observed with the Polariscope matched the strains observed with diphenyl oxide after the 150°C cure. Because of the progress with filled Doryl, further investigation of epoxy was terminated.

3. Low Temperature Glass

The glass frits were received in a powdered state. All of the powders were fine enough to pass through 200 mesh and some were specially ground to pass through 325 mesh. The finer powder improved the screenability, to a degree, however, even the coarsest powder performed satisfactorily. Acting upon the recommendation of Corning*, Squeegee Oil K595** was used to formulate the glass to a paste consistency. One advantage of this material is that storage in a closed container is feasible for long periods of time because the oil is not extremely volatile. Very little experimentation was required to find the proper screening consistency.

A microscope was mounted over a hot stage so that the glass could be observed during the maturing and cooling cycle. A variac in series controlled heating rates. The cooling cycle was really the most important of all because failures, if they would occur at all, occurred then.

After screening the specimens were prebaked at a temperature high enough to drive off most of the vehicle (125°C). The glasses were rapidly brought up to the temperature at which they vitrify and held there until matured. As indicated in a previous section, the devitrified types take a longer time to mature. The vitrified types can be started down the cooling cycle immediately after the powder converted to a glaze.

D. Preliminary Tests

1. Test Procedure

The samples were heated for more than 10 minutes at +125°C in an oven, air quenched for up to 30 seconds and then plunged into a dry ice and acetone bath, drying in air briefly, and returning to the oven at +125°C.

Since the stress in the substrates, chips, and filler material was peculiar to the geometry used, all the conclusive thermal shock testing was done using chips mounted in the substrates using the screening and curing techniques appropriate for that material. A typical test sample is shown in Figure 4-5. Many substrates were examined for stress before and

*Private correspondence from Dr. Robert Dalton.

**Dupont, Philadelphia, Pennsylvania.

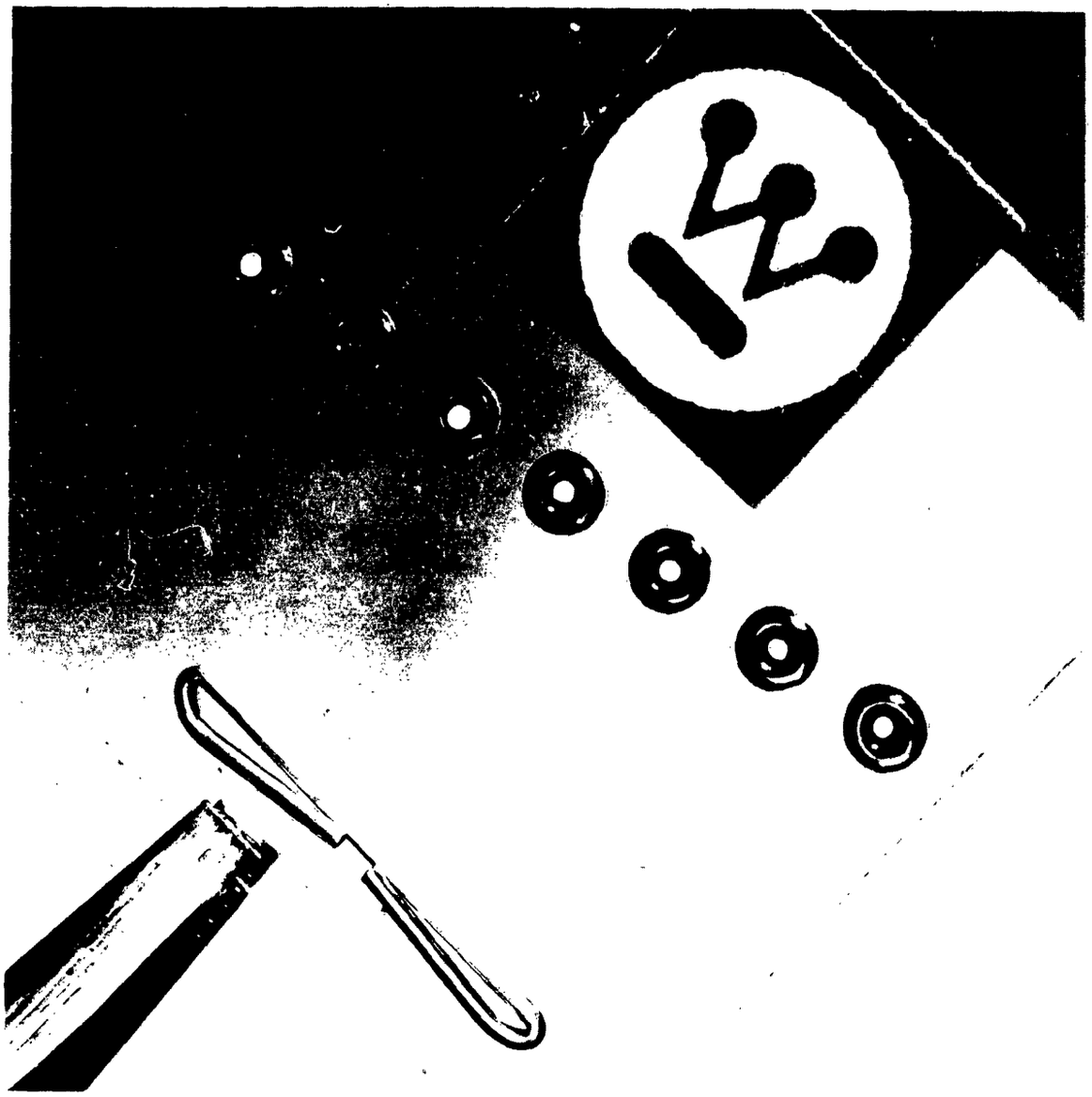

Figure 4-5

Test Sample Used to Evaluate
Bridging Material

after thermal shock using a Polariscope made by Polarizing Instrument Company, Inc., Mt. Kisco, New York. The effect of thermal shock has been evaluated by visual inspection for cracks in substrate, filler, or chips and measurement of resistance of conductors deposited over a series of substrate-filler-chip bridges. Both of these methods of evaluation were applied before and after thermal shock to the diphenyl oxide Resiweld 7004, and the low temperature glass systems.

2. Test Results

Table 4-11 lists the results of examination at 30 X magnification after fabrication of test samples. Evaluations were made on test samples typical of the specimen in Figure 4-5. The alumina-filled Doryl was cured at 150°C. Observations under the Polariscope examination of the A combination of Table 4-11 showed stresses in chip area comparing favorably in magnitude with E through J combinations. The B combinations showed extremely large stresses circumferentially around the chip. These observations, within reasonable limits, compared favorably with the results revealed by the microscope, i.e. specimens with visible failures showed the most intense stresses under the polariscope.

a. Inorganic Bridging Material

The only inorganic samples without visible failures after fabrication were in set A. After five cycles of thermal shock two of these sustained cracks in the substrate. The others, with some visible cracks to begin with, deteriorated progressively with each cycle at the -65°C quench. Based on these results a decision was made to drop the inorganic bridging material study.

b. Organic Bridging Material

All of the organic samples passed visual inspection after ten thermal cycles. Chrome-gold conductors were then deposited on 24 of the organic samples. Five alumina substrates in this group, accidentally overheated during deposition of conductors, showed catastrophic failure of conductors. The 19 good substrates included some with permutations the same as those which were overheated, showed less than five percent resistance change after thermal shock. This change is within a comfortable margin of the 10 percent resistance change from initial value requirement of SCL-7658B.

Table 4-11

Test Samples After Fabrication

Number of Samples	Permutation	Part 1	Part 2	Substrate	Bridging Material	Results
4	A	Corning 0211	Corning 0211	Corning 0211	Pyroceram 95	No visible cracks.
4	B	Silicon	Silicon	Corning 0211	Pyroceram 95	Circumferential crack in substrate; cracks in bridging material.
4	C	Corning 0211	Corning 0211	Alumina*	Pyroceram 95	All but one showed cracks.
4	D	Silicon	Silicon	Alumina*	Pyroceram 95	All but one showed cracks.
4	E	Corning 0211	Corning 0211	Corning 0211	Alumina-filled Doryl	No cracks.
4	F	Silicon	Silicon	Corning 0211	Alumina-filled Doryl	No cracks.
4	G	Corning 0211	Corning 0211	Alumina*	Alumina-filled Doryl	No cracks.
4	H	Silicon	Silicon	Alumina*	Alumina-filled Doryl	No cracks.
4	I	Silicon	Silicon	Corning 7740	Alumina-filled Doryl	No cracks.
4	J	Corning 0211	Corning 0211	Corning 7740	Alumina-filled Doryl	No cracks.

*Al Si Mag 614, American Lava Corporation, Chattanooga, Tennessee.

On the basis of the above results alumina filled Doryl was tentatively selected as the candidate bridging material for the model fabrication program. Although the preliminary tests proved rather conclusively that the process selected was satisfactory for the round chip there was still a question in the minds of all concerned with regard to the feasibility of this process for a square chip such as is called for in Task B. This led to the following test.

c. Square Chip Test

A simple experiment to determine the effect of mounting square chips in square perforations was conducted. Two samples of alumina-filled bridging material were employed.

Impact grinding techniques were used to grind 0.010 inch deep perforations into Corning 0211 glass substrates. Square silicon chips were made by scribing the sheet silicon and carefully breaking along the scribe lines. The chips were mounted into the square holes per the normal procedure and the bridging material was then applied manually under 30 X magnification, and cured. After five thermal cycles, there was an indication in some of the specimens of cracks at the corners of the bridging material. After ten cycles definite identification of cracks was made. A decision was then made to investigate fillers having a lower coefficient of thermal expansion than the aluminum oxide used in the existing formulation.

d. Zerifac-Filled Doryl Program

As result of a survey, Zerifac,* lithium silicate ($Li_2 O Al_2 O_3 \cdot 8 Si O_2$), was found to fit this description. It is an inert mineral filler having an essentially zero coefficient of thermal expansion. Zerifac has been used in resin systems as a means of providing good electrical properties, low average coefficient of thermal expansion, and high thermal stability, while keeping the specific gravity of the system low. It has the following properties:

*Manufactured by the Foote Mineral Company, Exton, Pennsylvania.

Table 4-12

Properties of Zerifac

Color	White
Linear Coefficient of Thermal Expansion (25-300°C)	-0.13×10^{-6} in/in/°C
pH (in water slurry)	9.05

Zerifac is thermally stable to 1260°C and its chemical inertness permits stable resin systems having excellent durability and weathering characteristics.

Table 4-13

Zerifac-Filled Doryl Formulation

The following formulation was developed after several screening trials:

Ingredients	Parts, by Weight
Diphenyl Oxide (B-109-3)	37.4
Cab-O-Sil Thixotroping Agent	0.6
Zerifac, 325 Mesh	40.0

As in the original formulation the viscosity of the base diphenyl oxide was controlled at 435 ± cps at 25 ± 1°C (Brookfield Viscometer, No. 1 Spindle at 20 RPM). The formulation was ball milled 24 hours to assure proper filler wetting and dispersion. This method of compounding also minimized air entrapment which occurs with many other compounding methods.

A cure was established for this compound as follows: A minimum of two hours at room temperature followed by one hour at 50°C, 65°C,

85°C, 100°C, 125°C, 175°C and finally two hours at 200°C. This schedule was essential to provide gradual solvent release from the compound and to extend its high temperature properties.

Samples were prepared for thermal shock testing with two substrates each of all permutations of Corning 0211 or silicon chips in Corning 0211, Corning 7740, or alumina substrates, using Zerifac-filled Doryl as bridging material. Examination under 30 X prior to thermal shock testing showed no cracking. Ten thermal shock cycles caused no changes except some of the Corning 7740 substrates showed cracking in the substrate between the fifth and tenth cycle. Examination under polarized light showed strains equivalent to those observed in the alumina-filled Doryl samples. Of significance are the respective curing temperatures which were for 200°C Zerifac-filled Doryl and 150°C for alumina-filled Doryl.

Four Corning 0211 substrates with square holes and square silicon chips were fabricated using Zerifac-filled Doryl. Two were cured to 150°C (for comparison with the previous 150°C cured alumina-filled Doryl with square chips) and two were cured at 200°C. All four showed no cracking after ten thermal shock cycles. Examination under polarized light showed slight strains comparable to those observed in 150°C cured alumina-filled Doryl bridging material.

On the basis of these results, Zerifac-filled Doryl was chosen as the bridging material for models, and additional efforts to improve screening were undertaken. To improve the screenability a super-fine grade of Zerifac was made by screening through a 400 mesh screen followed by ball milling for a total time of 72 hours.

e. Beta Eucryptite Filler

Some preliminary evaluation was made of Doryl filled with Beta Eucryptite ($Li_2O \cdot Al_2O_3 \cdot 2\,SiO_2$). The results indicated that this may also have promise because of its negative coefficient of thermal expansion, however, since Zerifac-filled Doryl was selected for the fabrication of models, a complete evaluation of Beta Eucryptite-filled Doryl was not conducted.

f. Side Experiments

There were a few side experiments. None were impressive enough to alter the decision made to use the Zerifac-filled Doryl, however, they are presented because of their relation to the program.

Beta Eucryptite was tried on some of the lower temperature glasses. There was some indication of a lowering of thermal expansion but not enough to alter our previous decision.

Brass chips were mounted in Corning 0211 substrates using Pyroceram 95. Cracking of the substrate resulted.

4.1.3 Substrate and Dummy Component Fabrication

A. Chip

Chips, 0.050 inch in diameter were fabricated using ultrasonic impact grinding techniuqes. Boron Carbide,* 280 mesh size, was used as the grinding compound. Choice of thickness of chips was based on availability. The typical silicon chip used by the Solid State Laboratory ranges from 0.003 to 0.010 inch in thickness. Corning 0211 glass sheets were available in thicknesses ranging from 0.003 to 0.024 inch. A nominal thickness of 0.010 inch was, therefore, considered representative for the chips. Since Task A was to establish feasibility of bridging disparities in vertical alignment as large as $\pm$ 0.005 inch, chips 0.005 and 0.015 inch thick were also considered. Chips were cut from scrap silicon wafers and Corning 0211 glass using ultrasonic impact grinding techniques and hollow tubes for drills. Figure 4-6 shows a typical head designed to fabricate 25 circular chips at a time. The glass chips measured from 0.050 to 0.055 inch in diameter and silicon from 0.048 to 050 inch. Considering the displacement allowed for the chip in the hole (Figure 4-7), these measurements are considered to be well within dimensions that can be tolerated.

B. Substrate

Perforations were cut into the substrates approximately 0;010 inch deep to within a 0.001 inch tolerance on 1/8 inch centers using

*Sold under tradename of Norbide by Norton Company, Worcester, Massachusetts.

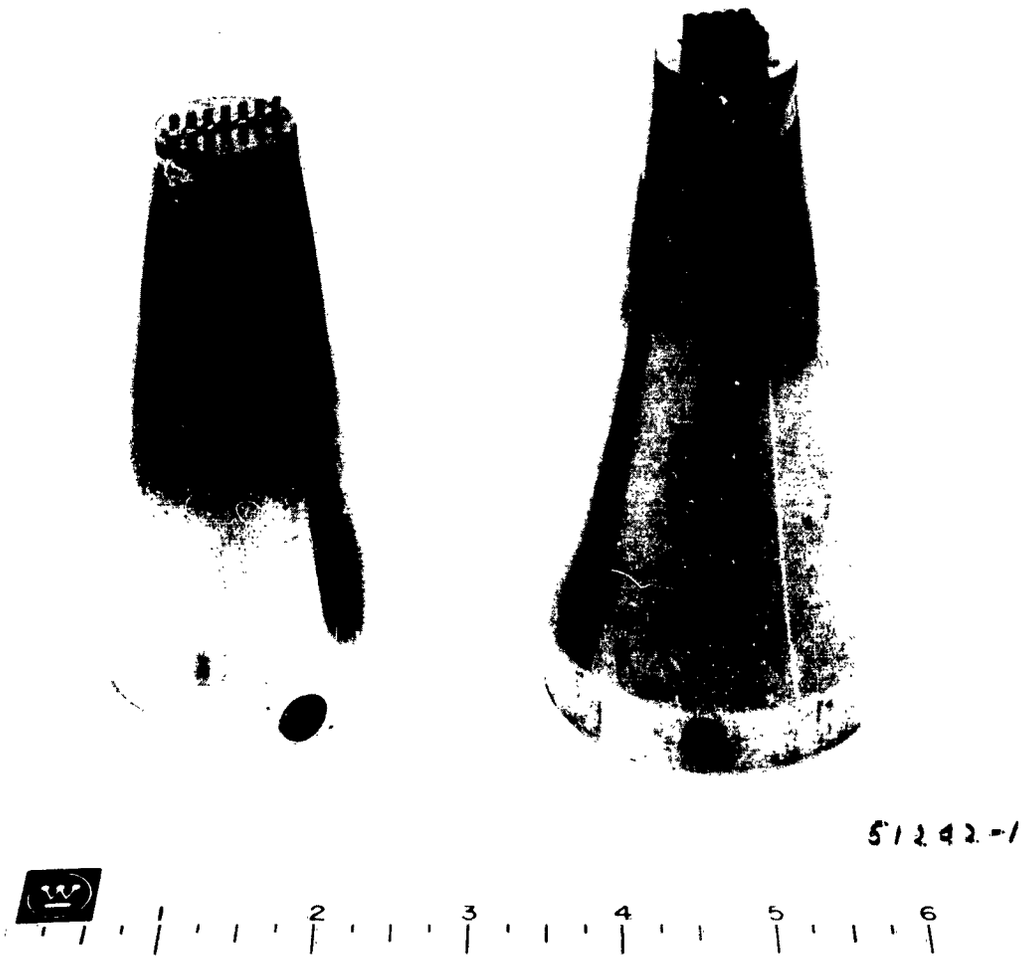

Figure 4-6. Impact Grinding Heads

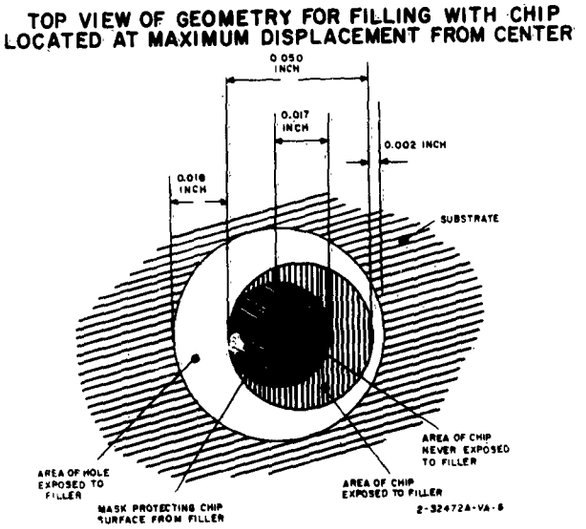

Figure 4-7. Top View of Geometry for Filling with Chip Located At Maximum Displacement from Center

ultrasonic impact grinding techniques. The diameter of the holes was fixed by the requirement that materials and techniques shall be capable of bridging gaps 0.018 inch maximum between terminal areas. With the chip diameter fixed at 0.050 inch, the hole diameter was calculated to be 0.070 inch. Drill stock, 1/16" OD, was selected for the grinding tool because it came closest to the dimension desired. The drilled holes actually measured 0.066 to 0.068 inch in diameter for the holes in 7740 glass and 0.066 to 0.070 for 0211 glass. The same drills cut 0.065 inch holes in unglazed alumina. From these observations, one concludes that hardness of material also influences to a degree the tolerances of impact grinding, however, these variations are relatively minor and are well within specifications. Depth of hole was held to $\pm$ 0.003 for the 0.010 inch hole.

C. Impact Grinding Head

The impact grinding head shown on the left of Figure 4-6 was designed for drilling the substrates for the test models. For the model fabrication, the design was changed to ten pins spaced so that two sets of experimental models were drilled at a time.

D. Substrate Jig for Models

A special jig was built to hold and register substrates for drilling the substrates for the models. The substrates arrived at the drilling table sized to fit the magazine of the microcircuit jig and waxed on a square templet. Many of these templets were made up ahead of time so that the drilling operation proceeded without interruption. The squared edge of the templet was registered to the squared edge of the substrate jig. All measurements were referenced to this corner. Permanently drilled in the jig was a set of holes matched to the grinding head and parallel to the reference edges. The center of the pattern was also lined up along one of the center-lines of the substrate. Once the operator attached the jig to his machine and aligned his table parallel to the reference lines he could accurately crank in the travel required to hit the geometric center of the substrate. Since the squared substrates were mounted on squared templets, the substrates were easily mounted with accuracy on the jig. Four patterns were drilled symmetrically about the center along cartesian coordinates. A jig having the precise dimensions of the mask changer was built to check sized substrates.

4.1.4 Thin Film Deposition Technique

A. Microcircuit Jig

1. Description

A microcircuit jig (Figure 4-8)* was installed in the vacuum system that was used for depositing metal film conductors in accordance with SCL-7638B. The unit, designed to produce multiple evaporations and mask changes without breaking the vacuum, held registration for each successive mask and substrate to within ± 0.001 inch. This control of placement of deposited connections met requirements of SCL-7638B. Facilities to ion bombard and heat substrates were also provided.

The jig contained two main parts, an upper and lower circular plate. The upper plate is a magazine capable of holding six 2" x 2" x 1/16" substrates. The lower plate is equipped to hold six masks. The thermal evaporation source also has six positions with its own indexing mechanism actuated by an external hand wheel. A second handwheel changes the masks and plates. Clockwise rotation of this latter handwheel first lowers the mask carrier away from the substrate plate and then moves the next mask into position. Counter-clockwise rotation raises the mask carrier and locates the selected mask in intimate contact with the substrate.

2. Mechanical Problems

a. Alignment Cone

Fouling of the alignment cone was found to occur from buildup around the cone by the deposited metal films. Disassembly of the magazines was necessary in order to clean and polish the cone to restore operation. Corrective action was accomplished by means of a modification of the shield to protect the cone from metal film deposits.

b. Timing Gear

Jamming of the substrate magazine occurred during the first few runs after installation. Disassembly of the jig revealed that the timing gear had slipped out of timing because the set screw was not secured properly.

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*Manufactured by Edwards High Vacuum, Inc., 3279 Grand Island Boulevard, Grand Island, New York.

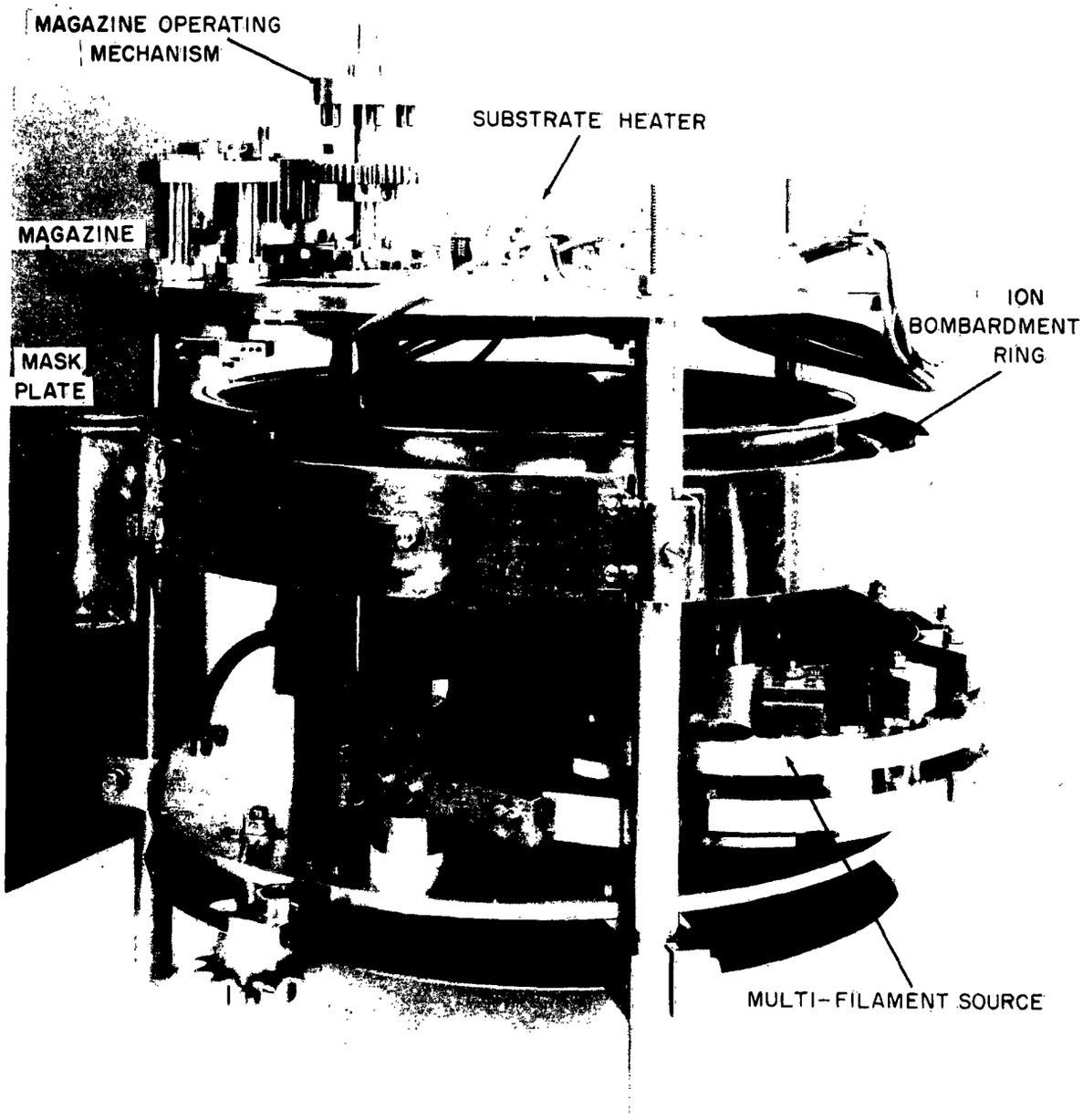

Figure 4-8. Microcircuit Jig

c. Galling of Multi-Filament Contacts

Due to the high current drawn by the multi-source copper turret, these parts were still very hot when exposed to air, and became oxidized as a consequence. This formation was serious enough to produce galling of the electrical contact surfaces. To eliminate this problem, an inert gas such as argon was used to break the vacuum. The oxidized surfaces were removed by rubbing with abrasive paper between runs. This approach was considered to be the most practical for a quick fix. A more permanent approach would be to form a protective coating on the bearing surfaces. Tin was tried on one of the two contact shoes without any significant improvement.

d. Miscellaneous

A standardized dimension and shape of boat was found to improve performance and lifetime of the boat for given charge and current. The dimensions before bending are 5/8" x 2 1/4".

B. Masks for Pads and Interconnections

In Figure 4-9 are shown the mechanical masks that were used to make models. Eight models were made per 2" x 2" slide. The 2" x 2" slides to the right of the masks illustrate typical patterns. The two smaller holes located on the periphery of the 2" x 2" area of mask fit into alignment pins on the microcircuit jig for registration. The masks were made from stainless steel sheet approximately 0.020 inch thick. The top mask is for the substrate terminal area and the lower one is for the interconnection pattern.

The pad mask was cleaned to remove film buildup every six cycles or every time the chamber was opened, whichever occurred first. The interconnection mask was cleaned between each deposition.

The interconnection mask was made by sawing eight 0.605 inch slots 0.006 inch wide. To provide for separation of the conductors over the chips, gold wire was pressed into slits less than 0.010 inch wide which were sawed at right angles to the 0.605 inch slots. These cross cuts are not visible in the photograph because they are on the backside of the mask.

SCL-7638B specifies that surface area of deposited interconnection shall not be greater than 0.006 inch in width and may range from 0.020 inch to 0.050 inch in length. Patterns obtained with this mask were in compliance with SCL-7638B.

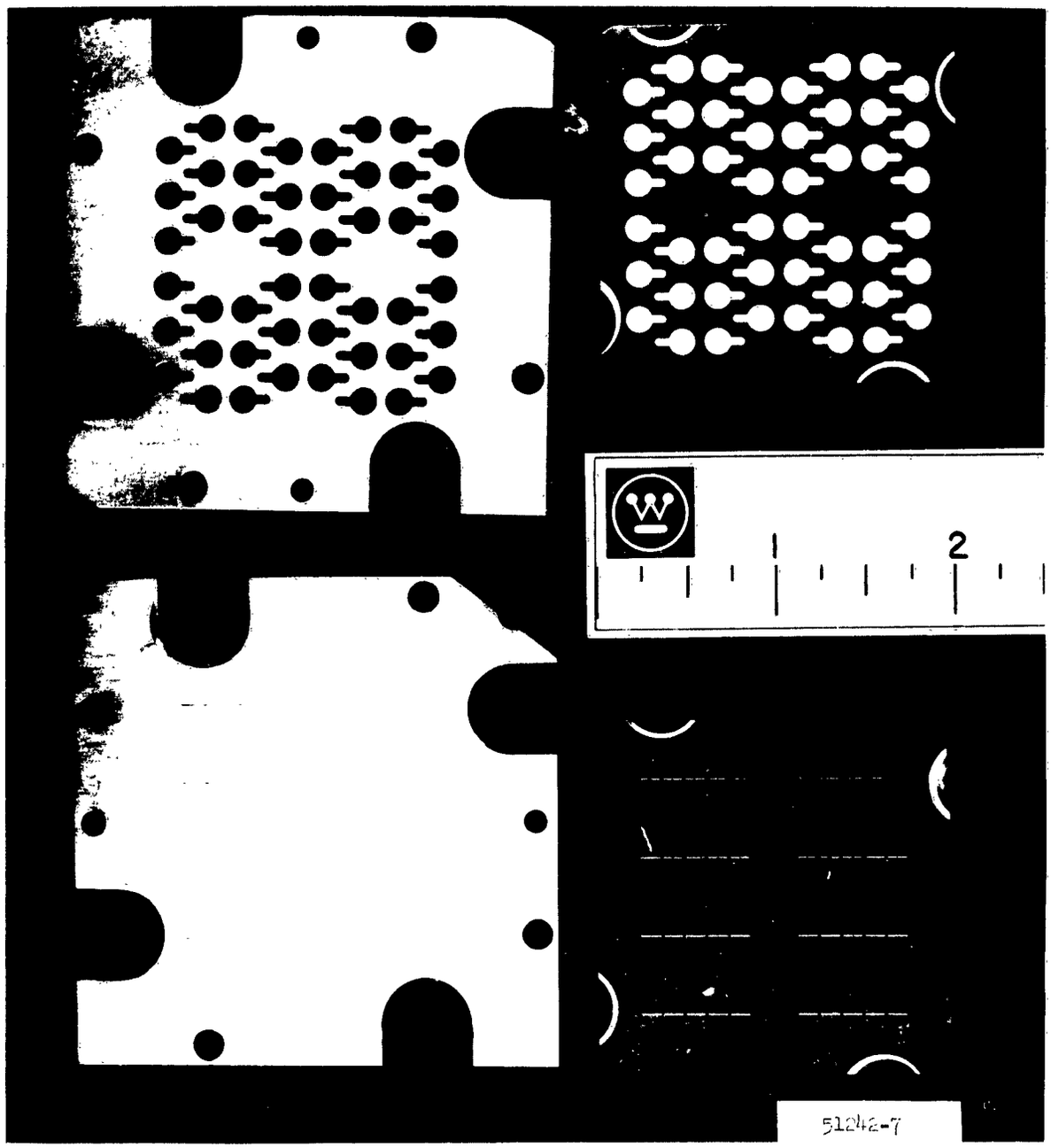

Figure 4-9

Mechanical Masks for Microcircuit Jig on Left.
Typical Patterns on Right.

C. Processes

1. Flow Diagram

The operations required to fabricate experimental models may be more easily followed by referring to Figure 4-10 which charts the process flow. The substrates were first sorted and sized in order to fit in the substrate magazine of the microcircuit jig. After impact grinding, the substrates were separated from the templets by heating on a hot plate. This softened the wax used used to hold the substrates to the templet. The soft wax was then removed by wiping and soaking in a solvent such as hot trichloroethylene. The substrates were then cleaned more rigorously as per Cleaning Procedure "A" given in detail by the flow chart in Figure 4-11. This process was followed by a chromic-sulfuric acid cleaning (Cleaning Process "B") which is detailed in Figure 4-12. A distinction in cleaning specifications was made here because of time sequence involved. In order to be effective, Cleaning Process "B" was done with no time elapse before the next step.

a. Pad Depositions

At first, the process flow followed the left hand branch, Figure 4-10, with pads (referred to as "terminal area on microwafer" in SCL-7638B) deposited after chips were mounted. Since the resin was only partially cured after chips were mounted the use of a drastic cleaning process such as chromic-sulfuric acid was precluded. As a result, the thin film pad adhesion was considered inadequate for reliability. By changing the sequence, as shown by the right branch, a much more practical situation resulted. This latter flow was adopted for all but a few of the early models.

b. Interconnect Depositions

After screening the bridging material, the models were subjected to a series of sprays of toluene, acetone, and alcohol using prepurified dry nitrogen gas for pressure and ending with iso-propyl alcohol vapors, as indicated in Figure 4-13.

A special process was developed to remove the oxidation product formed on the copper as result of exposure in air at the temperature required to cure the resin. This is shown in Figure 4-13, as the 1 percent hydorchloric acid etch rinses in water and alcohol respectively which preceded the organic sprays.

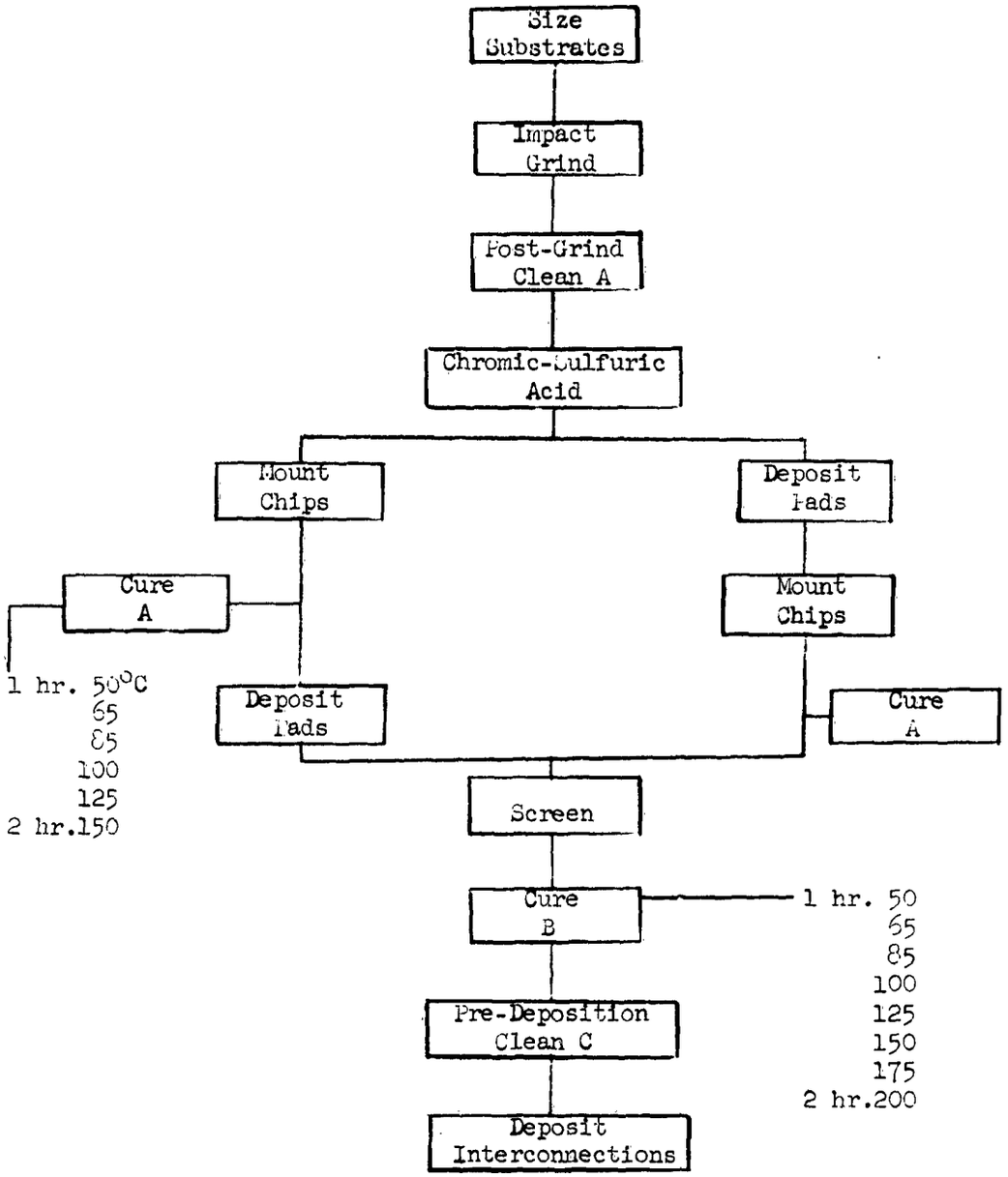

Figure 4-10. Fabrication of Experimental Models Flow Diagram

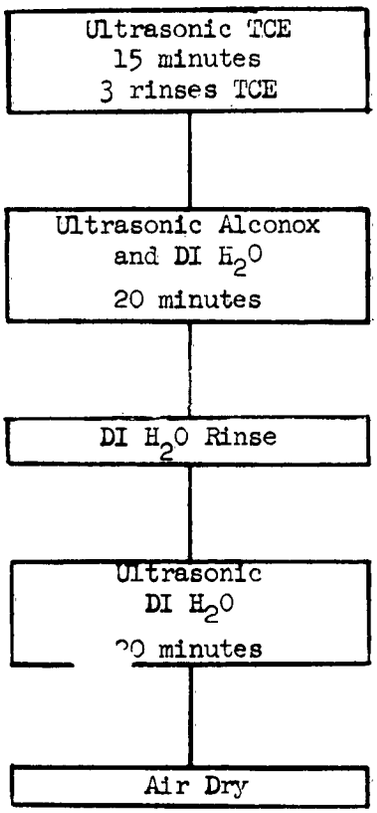

Figure 4-11. Post-Grind Cleaning Precedure A

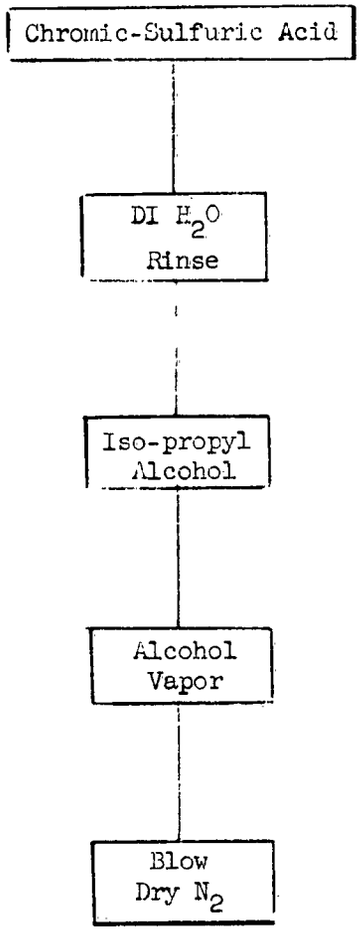

Figure 4-12. Acid Cleaning Process

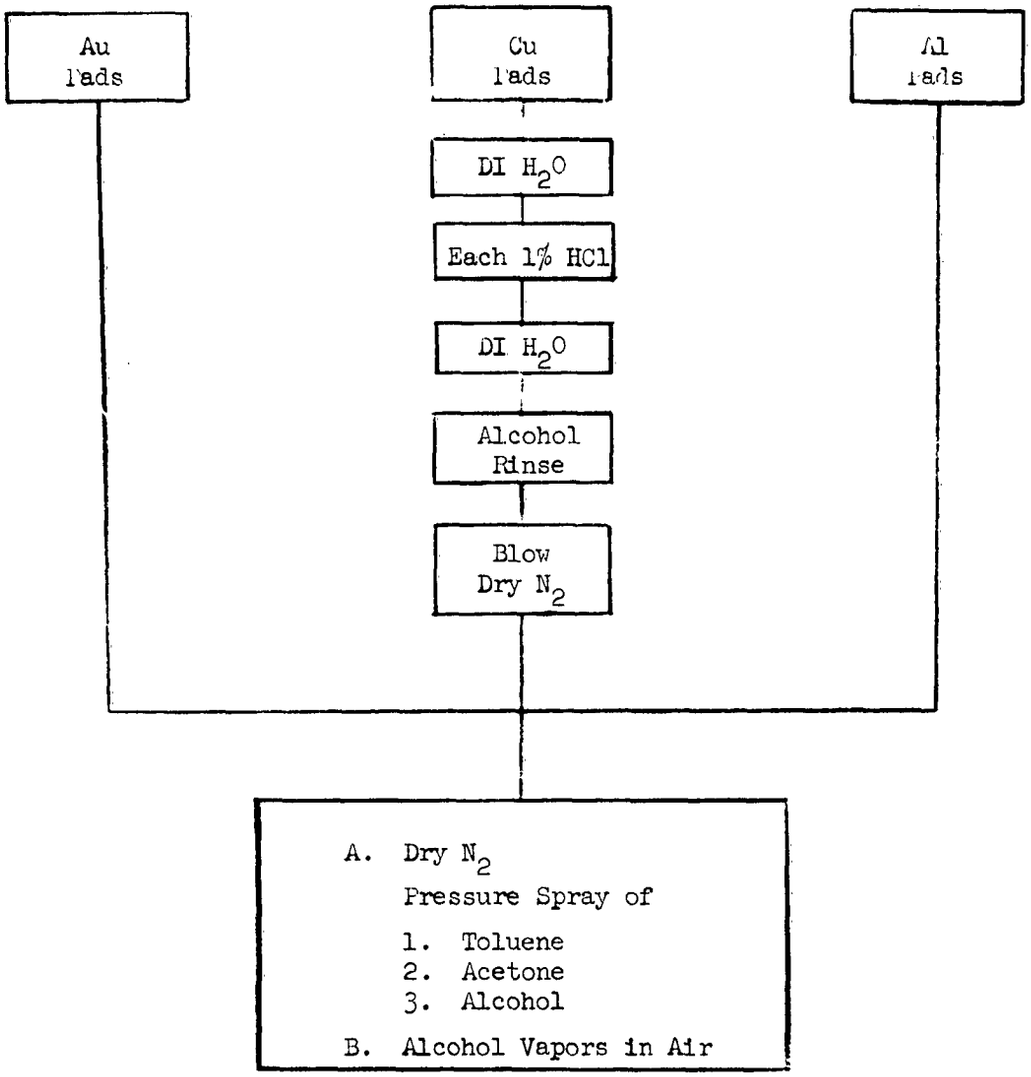

Figure 4-13

Pre-deposition of Interconnections;
Cleaning Procedure C

c. Deposition Parameters

The deposition parameters may be followed by referring to Figure 4-14. Heating was applied during pump down (minimum of 20 minutes). A pressure of less than 5×10^{-6} torr was reached before starting any of the sequence of operations.

The heat received during the pad evaporation differed from the interconnect evaporation for a fortuitous reason best explained by first describing the heating system design of the microcircuit jig.

One heater was located at the substrate slot over the active evaporation source. The slot adjacent to this position also had a heater which was wired in series with the other heater so that the temperature at this latter position was approximately half of the other. The purpose of this preheat design was to avoid a thermal shock to the substrates as they are brought into position to receive the evaporated film.

In the case of pad evaporations the full magazine load of six was run in series so that each substrate was preheated for a time equal to the time of heat during evaporation. The interconnect depositions, however, required so much metal, only one substrate was feasible during a single pump down. There was, therefore, no preheat, however, the actual evaporation was in most cases longer than required for the six pad evaporations so that the total heat was greater.

Heating was followed by 10 minutes of ion bombardment with argon gas. Since the system was fairly well outgassed after the first cycle, the ion bombardment time was reduced to five minutes for the cycles that followed, except when the jar was opened for any reason in which case the 10 minute cycle was once more resumed.

Since SCL-7638B called for capability of providing good electrical contact to clean terminal areas of gold, aluminum, and copper, these were the materials used for the pads. Chromium was used in all cases as a bonding film to improve adhesion. The chromium was deposited to a thickness that could be seen by inspection prior to deposition of the candidate metals.

Initial attempts to make interconnects of Cr-Au were short of meeting initial resistance specifications of SCL-7638B of 0.3 ohm per interconnection. To meet this specification with gold was considered

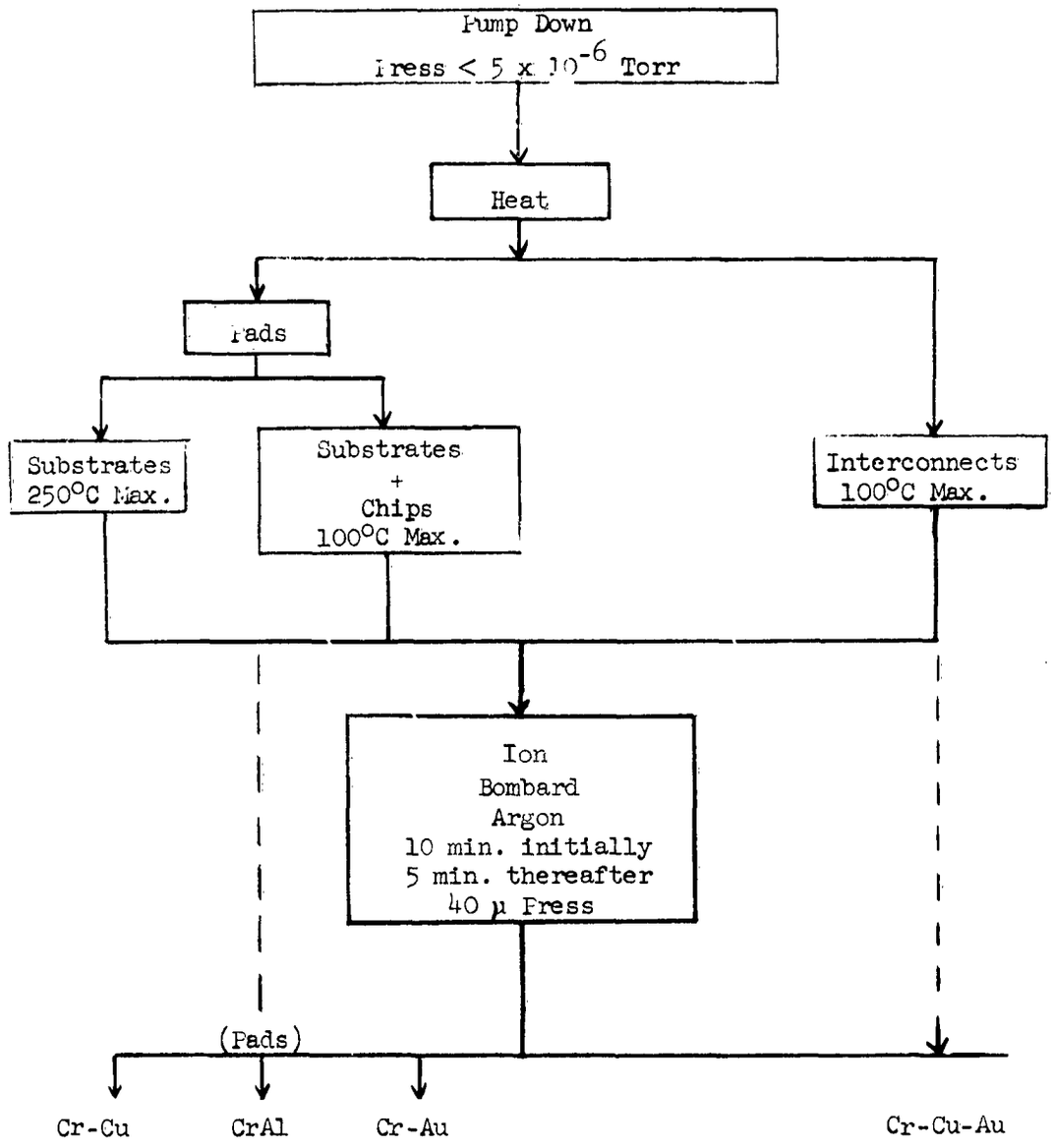

Figure 4-14. Flow Diagram for Deposition Parameters

economically unfeasible, therefore a decision was made to use copper to provide the bulk of the film. Gold, however, was still used for the final deposition. Four charges of copper were used per slide for interconnects on the early models, increasing to six on the later models in an attempt to improve yield. A single charge of Au was used per slide. If the vacuum system had to be opened for recharging the boats, gold was flashed on the interconnect to prevent oxidation of the copper. After closing the system, the complete deposition cycle was followed which included ion bombardment and chrome flash. Final conductor thickness was of the order of 0.4 mils, and required 2 1/2 to 3 hours for deposition.

d. Process Compatibility

The potential risk of oxidation of the metal pads during the curing cycles was not fully appreciated at the start of the program. Where oxidation effects were obvious such as for copper, the problem was resolved by etching down to the base metal. A much more subtle case, however was that of the aluminum. Because the oxide was virtually invisible, the effect was not detected until after the interconnects were made at which time the interconnects were found to be isolated electrically by the film of oxide formed over the aluminum pad. At this point all the models with pads had been made. In order to salvage the models with aluminum pads, approval was granted to metallize them with chrome gold. The pads and interconnects in this case were deposited without opening the chamber to atmosphere.

e. Resolution of Line Width

A very light discoloration was observed spreading beyond the width of the interconnect mask. This phenomena, however, was not observed with the pad deposition. The interconnect evaporation, as one may judge from the metal evaporated was very unusual. Of the three theories offered:

1. Copper diffusion
2. Rate of evaporation too high
3. Specular reflection of copper atoms which don't stick on first collision.

The least likely mechanism is number two.

It was concluded that there is a limit to the resolution for thick interconnects (resolution is defined here as the minimum spacing

before shorting of parallel conductors) as were made for this program.

4.1.5 Experimental Model Fabrication

A. Design of Experimental Models

SCL-7638B specified that experimental models shall consist of one or more pairs of 0.050 inch diameter metallized silicon or glass parts physically supported in microwafers. Provision shall be made for the permanent attachment of current and potential leads directly to the thin film terminations on the surface of the microcircuit wafer by a soldered connection in order to minimize variations in resistance that may result from measuring technique.

In the top illustration of Figure 4-15 is shown the plan view of the model. Visible are five small circles representative of chip areas. Two pairs of parts with a spare are seen available. The large pads are for permenent attachment of leads. The bottom illustration is a section view of the chip region to reveal in more detail the chip-bridging material-deposited interconnection interfaces. In actual practice, eight of these models were made on a 2" x 2" slide.

B. Fabrication

The technique of screening was found to improve with time. In fabrication of the test samples, the bridging material was screened through a 200 mesh screen.

In the process of scaling-up the screening operation to screening of 8 models simultaneously several minor problems were encountered. The flow of bridging material over the 2 x 2 inch area was not uniform enough to cover all the models. These problems were greatly alleviated with a larger mesh size screen fabricated by stretching and stapling a 124-mesh silk across a wooden frame. The surface characteristics this time, however, were degraded somewhat in the process. By trading-off surface characteristics against yield an optimum stainless steel screen of 164 mesh was finally selected. It was found necessary to use multiple screening passes to uniformly screen the majority of samples.

Screening is still a state of art even under these conditions. As experience was acquired, improvements in both quality, and,

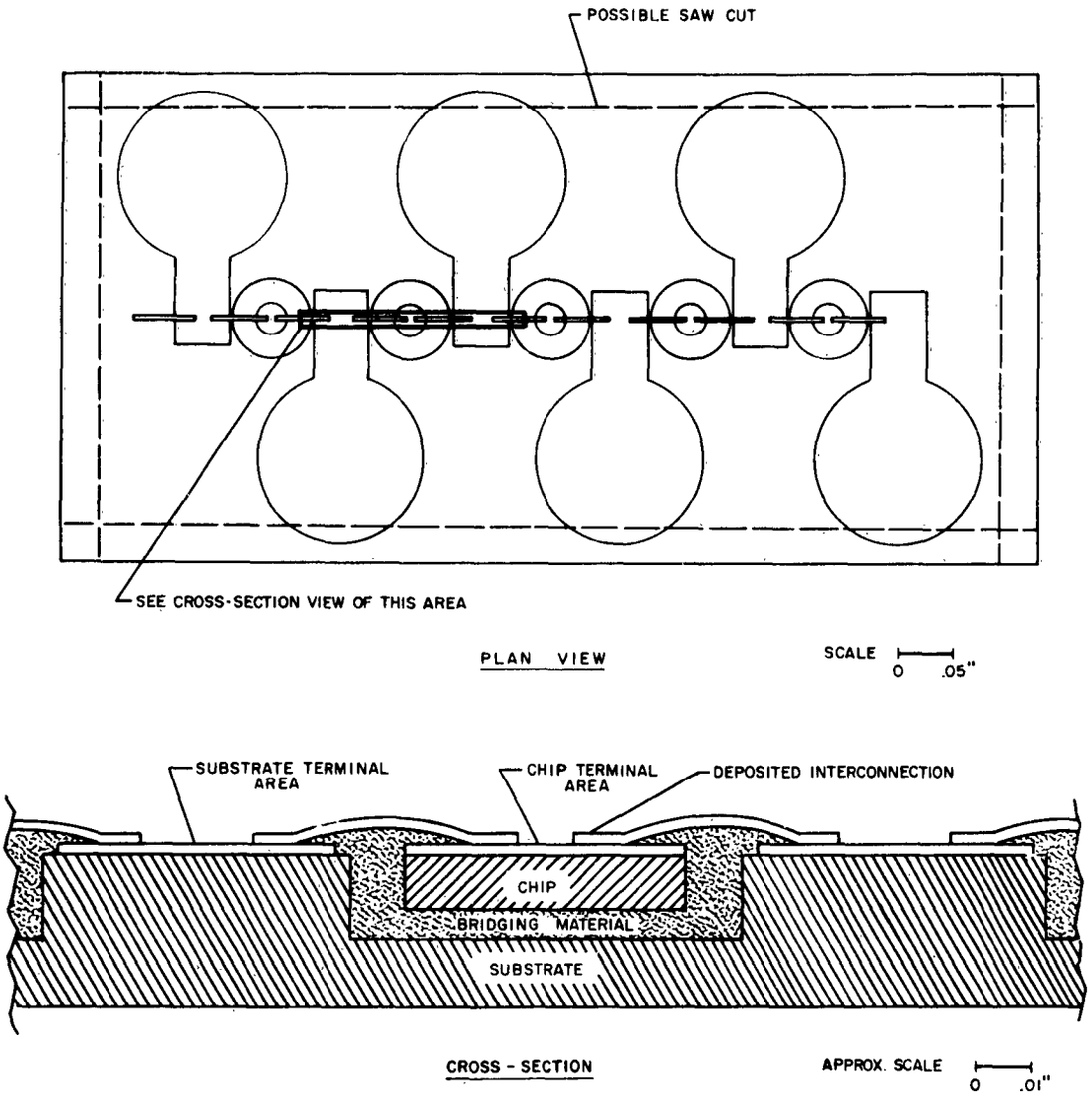

Figure 4-15. Experimental Models

increase in yield were found. As a result a nonuniformity in quality of the screened substrates was found, with the final runs of higher quality and more typical of production conditions.

A typical 2 x 2 inch slide containing eight experimental models is shown in Figure 4-16. The actual interconnect is shown in the circled enlargement. SCL-7638B required two or more pairs of metallized silicon or glass parts. In response to this requirement, five parts were actually supplied. Two pairs of deposited interconnections were used in resistance measurements out of each group of five pairs of interconnects.

Each group of 25 interconnection pairs, as listed in SCL-7638B was sub-divided into groups to include the different kinds of pads. The original distribution was 9, 8, 8 of gold, copper and aluminum, respectively. Because of poor adhesion found for the reworked aluminum pads on glass this permutation was replaced by gold pads. Table 4-14 shows the permutations finally used for models delivered as well as thermal shock tests. It will be noted that the 25 interconnection pairs on glass substrates were comprised of 17 pairs with gold pads and 8 with copper pads. The alumina substrates have the 9-8-8 combination cited previously.

4.1.6 Engineering Qualification

A. Preliminary Tests

One of the techniques used to guide our process was to modify the thermal cycle test specified by SCL-7638B, (given in Table 4-15) so as to yield an answer more expediently. In the method used, the time at room temperature was shortened from 5 minutes to 30 seconds, repeating ten cycles. A lower temperature of -79°C was used instead of -55°C.

Test results of round chips bridged with alumina-filled Doryl and low temperature glasses, summarized in Table 4-11, showed no cracks only for the alumina-filled Doryl. The same test applied to four square chips bridged with alumina-filled Doryl, on 0211 glass substrates, cracks were indicated in some of the specimens after five thermal cycles with definite identification of cracks after ten cycles. On the other hand four square chips bridged with Zerifac-filled Doryl on 0211 glass substrates passed ten thermal cycles without any visible signs of cracking. All

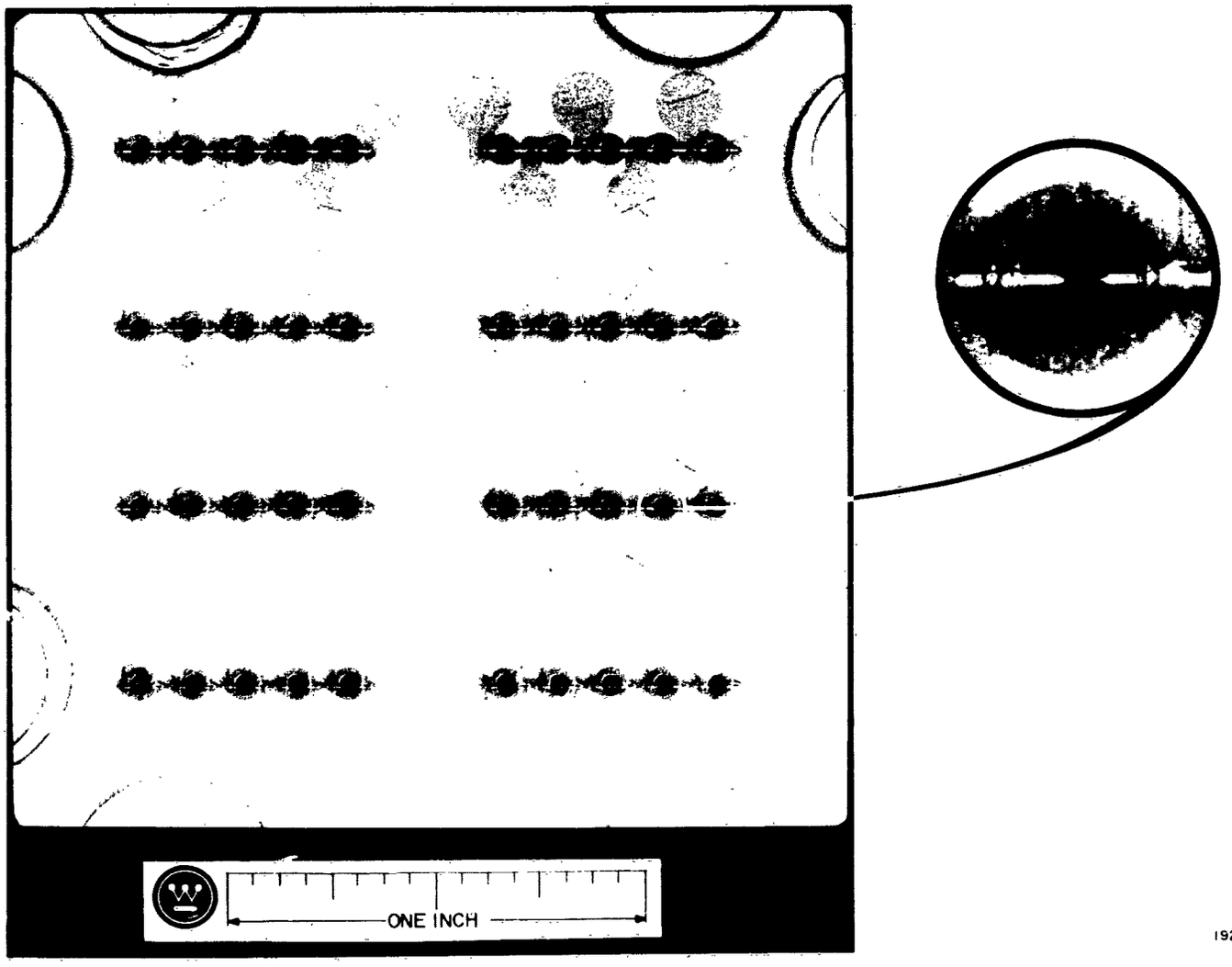

Figure 4-16. Typical 2 x 2 Inch Slide Containing Eight Experimental Models. A Pair of Interconnects is Illustrated in Magnified View.

TABLE 4-14

EXPERIMENTAL MODELS DELIVERED

Number of Interconnects	Parts	Substrate	Pad
17	Glass Glass	Glass	Au
8	GG	G	Cu
17	SS	G	Au
8	SS	G	Cu
17	GS	G	Au
8	GS	G	Cu
9	GG	Alumina	Au
8	GG	A	Cu
8	GG	A	Al
9	SS	A	Au
8	SS	A	Cu
8	SS	A	Al
9	GS	A	Au
8	GS	A	Cu
8	GS	A	Al

Total: 150
G = Glass: Corning 0211
A = Alumina: Alsimag 914
S = Silicon

Table 4-15
Thermal Cycle

Steps	Temperature (°C)	Time
1	$-65\ ^{+0}_{-5}$	10 minutes
2	$+25\ ^{+10}_{-5}$	5 minutes
3	$+125\ ^{+3}_{0}$	10 minutes
4	$+25\ ^{+10}_{0}$	5 minutes
5	Repeat steps 1 through 4 for a total of 100 cycles. Models may be stored at 25°C +10 -5 between cycles if required for convenience.	

observations for cracks were made at 30 X magnification.

To determine compatibility, chrome-gold conductors were deposited over Zerifac-filled Doryl and a control (soda lime glass). The conductors passed adhesion tests prescribed by SCL-7638B before and after thermal shock. Resistance data after one thermal cycle is listed in Table 4-16.

Table 4-16
Thermal Cycle Data on Zerifac-Filled Doryl

			Initial Resistance (ohms)	% Change After Thermal Shock
Sample 1	Conductor	on glass	0.9	2
		on bridging material	1.72	0.6
Sample 2	Conductor	on glass	1.73	0.6
		on bridging material	1.62	1.0

B. Adhesion Tests

SCL-7638B specified that the deposited interconnection on terminal areas shall be capable of withstanding a cellophane pressure sensitive adhesive tape firmly and evenly impressed on the surface and subsequently pulled at a right angle until removed from the surface. Twelve samples tested, covering all permutations, passed with the exception of reworked aluminum pads on glass. In this case poor adhesion was found between the oxidized aluminum and the chrome-gold. This discovery was unexplained because these same samples of reworked aluminum pads on glass showed excellent pad adhesion during resistance measurements.

Fifteen more experimental models tested after 100 thermal cycles per requirements of SCL-7638B passed adhesion tests. Samples of each of the six permutations of chip/substrate were once again represented in the selection.

Finally, twelve experimental models tested after 1000 hour low temperature storage passed adhesion tests. Once again all permutations were included in sampling.

C. Low Temperature Storage

SCL-7638B specified that 150 models shall be stored for 1000 hours at -55° with 99.7 percent having a percent-resistance-change-from initial value which shall not exceed 10 percent. Measurements of interconnection pair resistance were made prior to and at the end of 1000 hours storage. Appendix II lists the complete data for the measurements. Table 4-17 shows the number of interconnection pairs of each permutation of chip, pad and substrate tested.

Pairs were selected with resistances less than 0.6 ohm resistance prior to storage. Figure 4-17 is a plot of the change in mean resistance for each permutation shown in Table 4-17 after 1000 hours storage at -55°C. There were no catastrophic opens for interconnection pairs resulting this test.

D. Moisture Resistance

A preliminary moisture sample in a deposited comb pattern (Cr-Au conductors) over a screened strip of Zerifac-filled Doryl on a microscope slide corroded severely after a few days with a 90 volt bias voltage applied. A second sample, protected with DC-271 showed evidence of

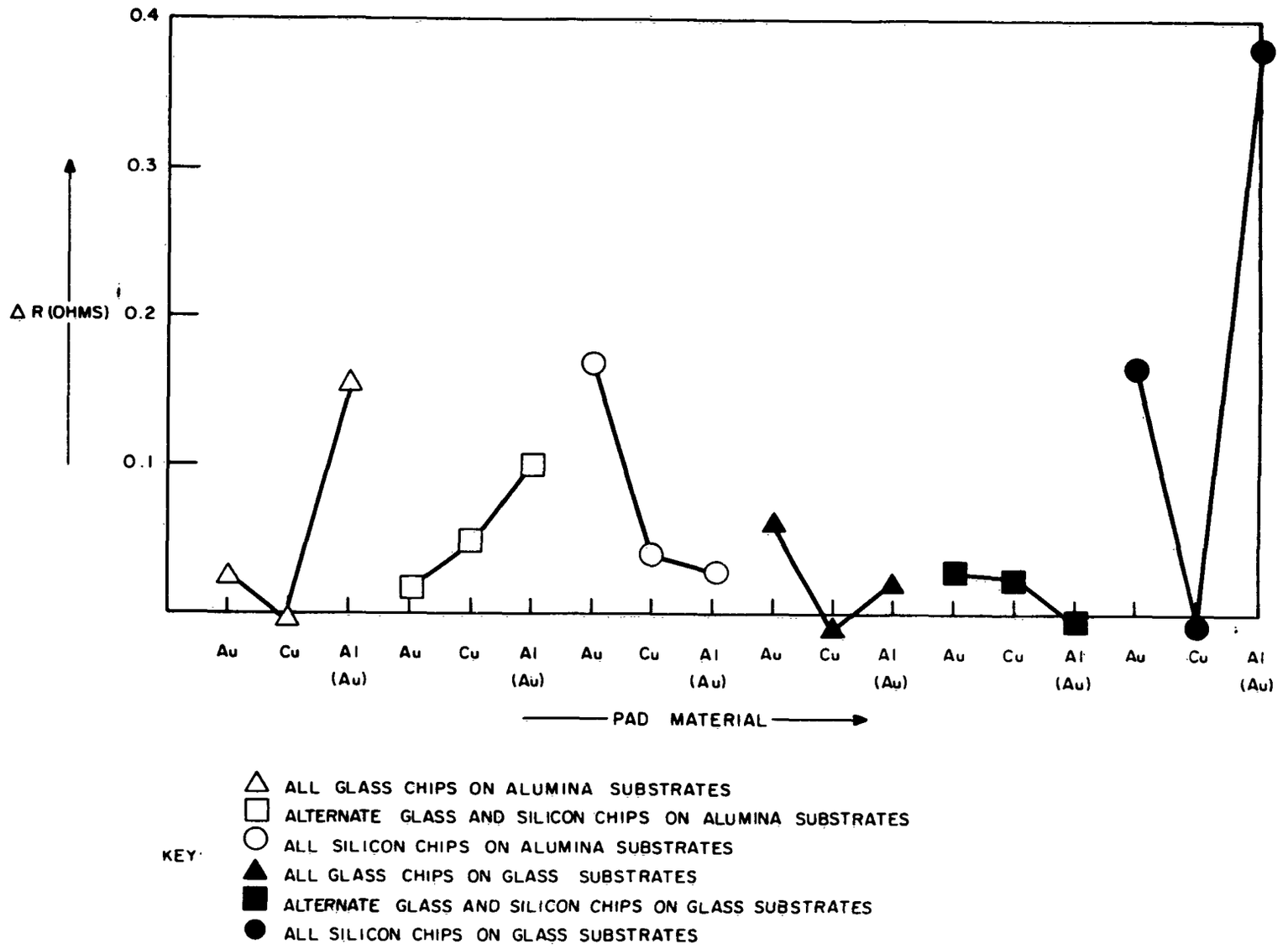

Figure 4-17. Resistance Change Due to Low Temperature Storage

Table 4-17

Low Temperature Storage Permutations

Permutation*	Interconnection Pairs	Permutation	Interconnection Pairs
GGA-Au	9	GGG-Au	9
GGA-Cu	8	GGG-Cu	8
GGA-Al (Au)*	8	GGG-Al (Au)*	8
GSA-Au	9	GSG-Au	9
GSA-Cu	8	GSG-Cu	8
GSA-Al (Au)*	8	GSG-Al (Au)*	8
SSA-Au	9	SSG-Au	9
SSA-Cu	8	SSG-Cu	8
SSA-Al (Au)*	8	SSG-Al (Au)*	8
Total	75		75

G = Glass: Corning 0211

A = Alumina: Al Si Mag 914

S = Silicon

*Reworked pad

corrosion of the conductor in areas where the DC-271 bubbled. The sample measured .01 percent of its initial resistance after test. Several days later the resistance returned to its initial value.

Figure 4-18 shows the final design used which was made in accordance with SCL-7638B. There are 20 parallel conductors, 0.006" wide, spaced 0.005" apart and 0.100" long. The samples were made by impact grinding slots approximately .010" wide and .010" deep in alumina substrates. An excess of bridging material was filled in the slots to allow for shrinkage during the cure through the 150°C. Toluene used with Q-tips to remove excessive material and sharp corners is believed to have retarded the cure because two extra hours at 200°C were required for a toluene resistant state.

The comb conductor pattern used in the moisture resistance test was deposited through a mechanical mask. The deposit of

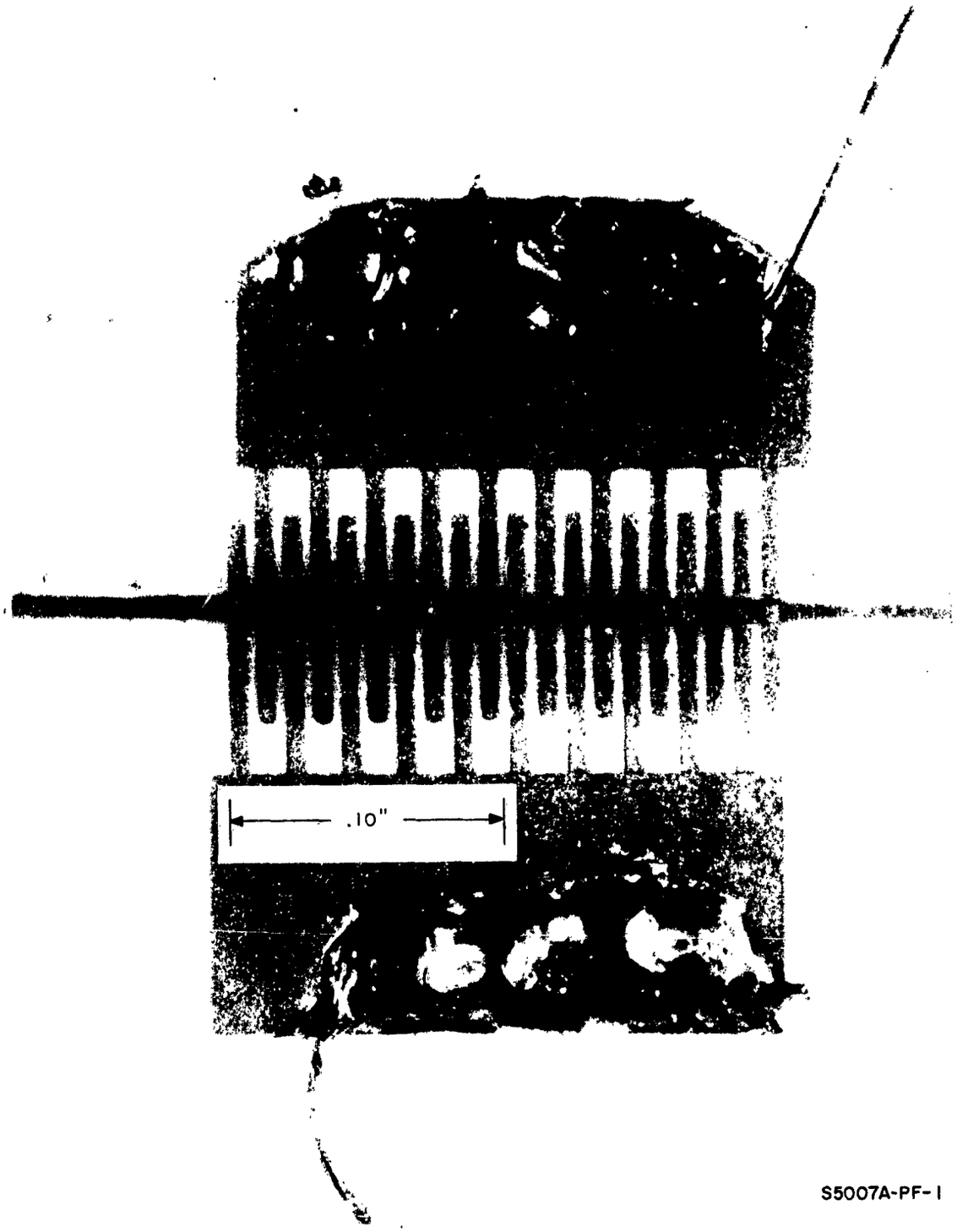

Figure 4-18. Test Sample for Moisture Resistance Test

chrome-copper-gold was of the order of 2 to 3 microns thick. Diluted Silastic 140* (7 parts 140 to 3 parts xylene by weight) was found to offer the best protection. It was cured in air at room temperature for 60 hours.

Table 4-18
Moisture Resistance Data

Sample No.	Initial Resistance (MΩ)	Final Resistance (MΩ)
1	> 200,000	27
2	1,500	5
3	> 200,000	6
4	7,000	45
5	> 200,000	70
6	2,800	300
7	> 200,000	1000
8	> 200,000	43
9	> 200.000	200
10	> 200,000	3

Figure 4-18 shows a typical test sample after ten days of humidity testing, and Table 4-18 shows test results.

E. Thermal Shock Test

SCL-7638B specified that the models shall meet the previously stated requirements of resistance measurements before and after 25, 50, 75 and 100 temperature cycles. Temperature cycling to be performed in accordance with Method 107 of MIL-STD-202, except that conditions shown in Table 4-15 shall apply. Table 4-19 shows the number of interconnection pairs of each permutation of chip, pad, and substrate tested.

Appendix I lists complete data for the thermal cycling resistance measurements. All interconnection pairs which underwent thermal

*Manufactured by Dow Corning.

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Sample No.	Initial Resistance (MΩ)	Final Resistance (MΩ)
1	> 200,000	27
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3	> 200,000	6
4	7,000	45
5	> 200,000	70
6	2,800	300
7	> 200,000	1000
8	> 200,000	43
9	> 200,000	200
10	> 200,000	3

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Appendix I lists complete data for the thermal cycling resistance measurements. All interconnection pairs which underwent thermal

*Manufactured by Dow Corning.

cycling were initially selected in order to have resistances less than 0.6 ohms before testing. Figure 4-19 is a plot of mean resistance change for each permutation shown in Table 4-18 after 25, 50, 75 and 100 thermal cycles, respectively. The limits indicated for each mean resistance change represent the standard deviation of the measurements for each permutation. The data shown in Figure 4-19 obviously does not include these interconnection pairs which failed under thermal cycling with resistances of infinity. It should be noted that there were no resistances between 12 ohms and infinity.

A summary of these catastrophic failures is shown in Table 4-20.

Table 4-19
Thermal Cycle Models

Number of Interconnects	Parts	Substrate	Pads
9	GG	A	Au
8	GG	A	Cu
8	GG	A	Al (Au)*
9	GS	A	Au
8	GS	A	Cu
8	GS	A	Al (Au)*
9	SS	A	Au
8	SS	A	Cu
8	SS	A	Al (Au)*
17	GG	G	Au
8	GG	G	Cu
17	GS	G	Au
8	GS	G	Cu
17	SS	G	Au
8	SS	G	Cu

Total: 150
G = Glass: Corning 0211
A = Alumina: Al Si Mag 914
S = Silicon
*Reworked Pad

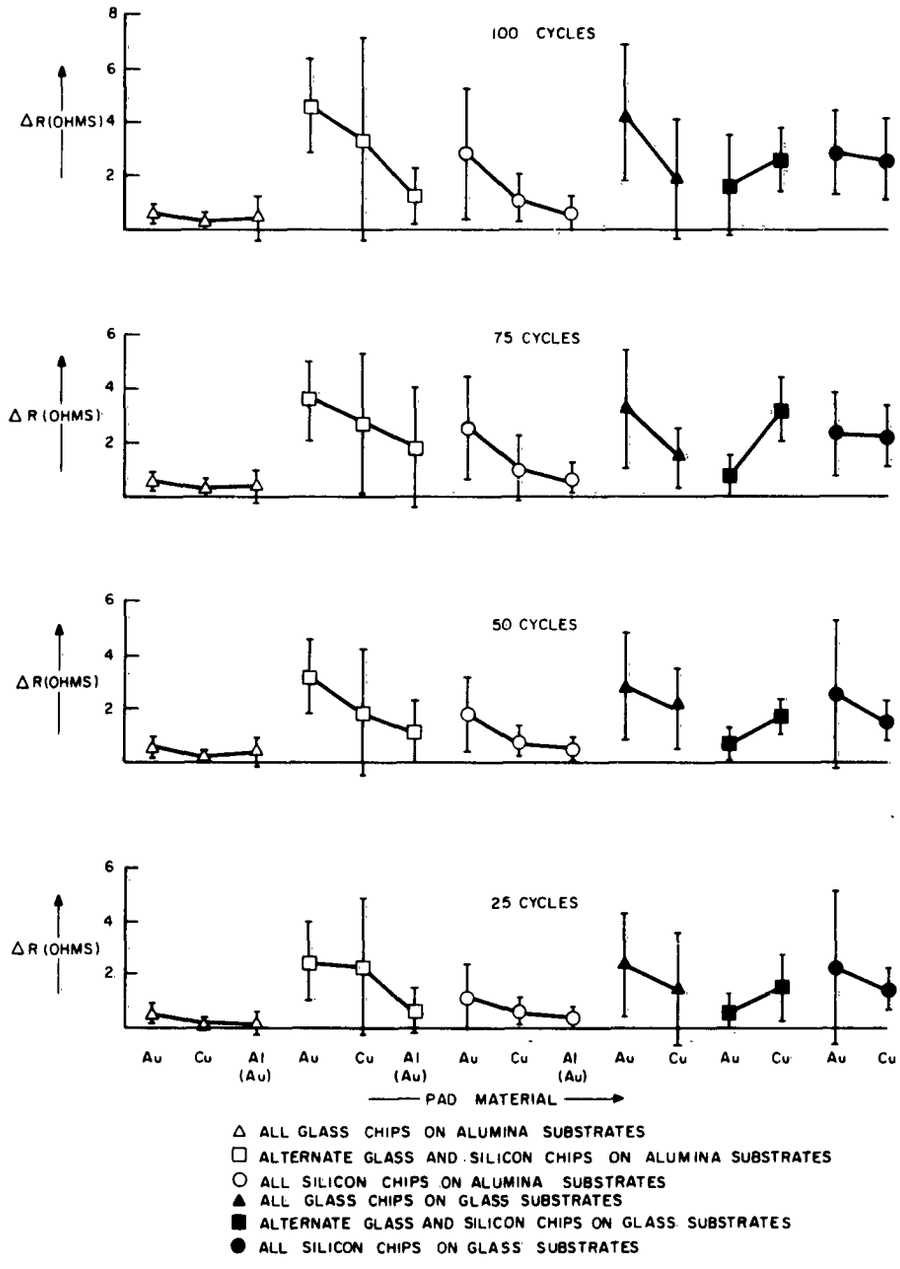

Figure 4-19. Resistance Change Due to Thermal Cycling

Table 4-20

Catastrophic Failure Models

Permutation* Parts Substrate-Pad	Number of Catastrophic Opens	Number of Substrates Involved	Number of Interconnects
GGA-Au	1	1	9
GGA-Cu	0	1	8
GGA-Al (Au)	0	1	8
GSA-Au	0	1	9
GSA-Cu	2	1	8
GSA-Al (Au)	0	1	8
SSA-Au	0	1	9
SSA-Cu	0	1	8
SSA-Al (Au)	2	1	8
GGG-Au	3	2	17
GGG-Cu	3	1	8
GSG-Au	0	2	17
GSG-Cu	3	1	8
SSG-Au	7	2	17
SSG-Cu	—	1	8
Totals	24	18	150

G = Glass: Corning 0211

A = Alumina: AlSiMag 914

S = Silicon

Examination of causes of catastrophic failure of interconnection pairs yielded the information summarized in Table 4-21.

Figure 4-20 shows an example of a substrate with poor adhesion at the junction between pad and interconnect conductor. A piece of 1/8 mil foil has been inserted between the pad and the conductor to

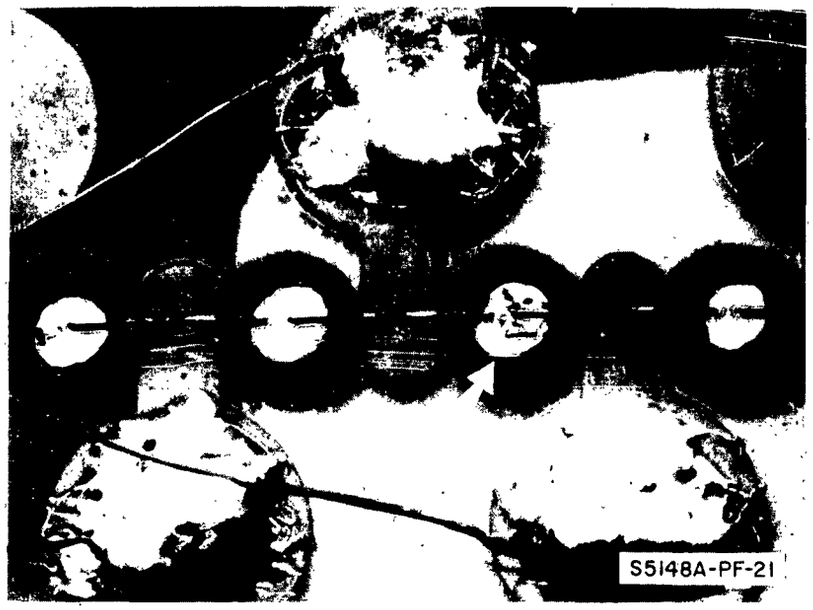

Figure 4-20. Poor Interconnect Adhesion with Foil Inserted Between Pad and Interconnect.

Figure 4-21. Interconnect Conductor Crossing Irregular Surface in Bridging Material

locate the break. Pushing down on the interconnect conductor with a probe causes visible motion of the conductor where this effect was identified as cause of failure. Figure 4-21 shows an example of an interconnect conductor crossing a sharply irregular surface in bridging material. Probing the conductor establishes the location of the break in these cases.

Table 4-21

Catastrophic Failures: Summary

Number of Opens	Cause
3	Poor adhesion observed at junction between pad and interconnect conductor.
8	Roughness or sharp irregularity in bridging material surface.
5	Mis-registration causes marginal area of contact between pad and interconnect conductor.
6	Failures of pad to substrate adhesion.
2	Continuous again (probably marginal pad to interconnect conductor adhesion).
24	Total

Table 4-22 shows the opens for substrates with rough or irregular bridging material surface finish versus smooth bridging material surface finish.

Table 4-22

Effect of Roughness on Opens

Bridging Material Finish	Number of Catastrophic Opens	Number of Substrates with Opens	Number of Substrates Without Opens
Smooth	11	4	7
Rough	13	5	2
Total	24	9	9

Figure 4-22 shows an example of mis-registration causing a marginal area of contact between pad and interconnect conductor.

4.1.7 Failure Mechanism Study

The principal reason for this study conducted after the formal environmental tests was to attempt to understand why there was a disagreement between the preliminary and final tests, and also, if possible, lay down a foundation for further development of a bridging material. The following observations resulted from an examination of the data.

A. Observations

1. Cracking of the filled Doryl and catastrophic opens in conductors appeared unrelated. Table 4-20 shows almost four times as many opens for glass substrates whereas Table 4-23 shows almost no cracking for glass substrates (actually only one case).

2. Examination of models on glass substrates in polarized light revealed no stresses around or near the chips for all models examined. This type of examination, unfortunately, is not applicable to opaque substrates such as alumina.

3. Slight cracking in filled Doryl almost always was radial whereas extensive cracking was circumferential (Table 4-24).

4. The cracking was independent of the chip combination (Table 4-23).

5. No chips were found cracked.

B. Interface Test

The consistency of the evidence of cracking as related to substrate, immediately aroused our suspicion that perhaps an interface effect was operating. To test this hypothesis a simple experiment was conducted consisting of a sandwich of alumina and glass bonded together with filled Doryl. This specimen was thermal shocked until separated. Failure occurring at the glass -- Doryl interface implied that this interface was weaker than the other. In terms of stress analysis, one may then conclude that failure was avoided in the glass substrate models because the stresses were relieved at the interface by a physical separation.

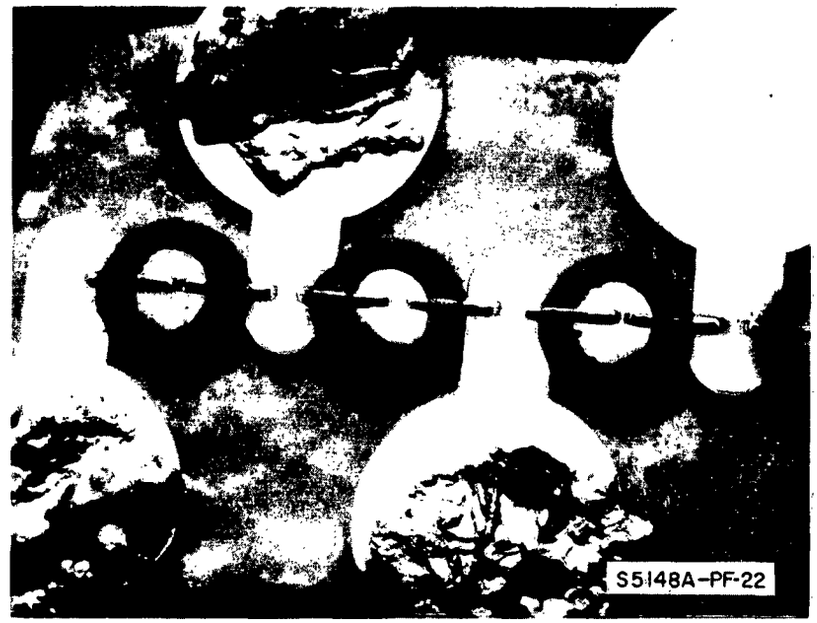

Figure 4-22. Marginal Area of Contact Between Pad and Interconnect Conductor Due to Misregistration of Masks

Table 4-23

Filled Doryl - After Thermal Cycles

Permutation Pad		Nature of Cracking				
		S	M	L	Radial	Circumferential
Part/Substrate	Pad					
GG/A	Au			X		X
GG/A	Cu	X			X	
GG/A	(Au)*	X			X	X
GS/A	Au					
GS/A	Cu		X			X
GS/A	Al (Au)			X		X
SS/A	Au			X		X
SS/A	Cu	X			X	
SS/A	Al (Au)	X			X	
GG/G	Au					
GG/G	Au	X			X	
GG/G	Cu					
GS/G	Au					
GS/G	Au					
GS/G	Cu					
SS/G	Au					
SS/G	Au					
SS/G	Cu					

G: Corning 0211

A: AlSiMag 614 manufactured by American Lava, Chattanooga, Tennessee.

* Reworked pad.

S: Slight

M: Medium

L: Extensive

C. Analysis of Radial vs. Circumferential Cracks

For all practical purposes all of the radial cracks were found around the chip edge. From our knowledge of stress analysis the radial cracks indicate a circumferential stress and the failure always is in tension. Since this is the smallest section of the bridging material, in the absence of any other unusual condition, this would be the most likely site for failure. When this failure does occur, it is noted that the stress is relieved in the area.

Following the same line of arguments, the circumferential cracks are due to radial stresses. This failure would have to be due to a radical change in the material characteristics so that cataclysmic failure would occur. Once again, after a crack has been propogated, the stress is relieved.

It is possible the two modes of cracking occur as a result of differences in degree of plastic deformation the bridging material undergoes. The radial cracking could be occurring in cases where a large part of the stress in the bulk of the filler is relieved through flow of the material. Thin sections of filler on top of the chips could be subjected to unusual stresses as a result of its inability to undergo plastic deformation as readily as the thicker sections in the gap.

D. Chemical Stability

Rather obvious was the difference in the shrinkage of the Doryl in the preliminary and experimental models. Although the available literature assured a high chemical stability, it still was considered advisable to confer with Dr. Sprengling of Westinghouse Research Laboratory (inventor of Doryl) on the probable effects of the various processes used. The ensuing discussion disclosed that there is 10 to 15 percent free diphenyl oxide in the cured resin which may be unstable in a vacuum environment. Such loss of diphenyl oxide very likely could leave the Doryl in a brittle state.

E. Summary and Conclusions

1. The difference noted for the preliminary tests and experimental models was due to an inherent instability of the Doryl which did not become obvious until it was exposed to the protracted vacuum cycles used for the models only. If the same processes had been more similar the

experimental models very likely would have passed the environmental tests.

2. The absence of filled-Doryl cracking on the glass substrates was due to a separation at the Doryl-glass interface.

Further thermal cycling of the original test samples used to evaluate the bridging material (cf page 4-5, 2nd quarterly report) showed these original samples withstood further thermal shock without cracking. To establish the difference between these original evaluation samples and the experimental models the processes used in fabricating the experimental models were re-examined. After noting that the original samples did not undergo the same vacuum deposition as the experimental models disparity became one of suspicion. As a result, an experiment to determine the effect of vacuum deposition processes on the bridging material was conducted. The results are shown in Table 4-24.

Table 4-24

Effect of Process Variables on Filled Doryl

Process / Test	Heat in Vacuum and Glow Discharge Cleaning and Solvent Cleaning	Solvent Cleaning	No Treatment
25 thermal cycles	30 samples no cracks	30 samples no cracks	20 samples no cracks
50 thermal cycles	20 samples 3 cracks	20 samples 1 crack	10 samples no cracks

Basically, the chemical structure of the resin can be represented as a diphenyloxide polymer with methylene bridges. The degree of functionality (and subsequent cross linking) and the average molecular weight can be modified by the initial reaction process leading to some variations in properties. Additionally, the particular reaction method currently employed leads to a residual, non-reacted, free diphenyl oxide concentration of 10 to 15 percent in the specific composition employed in this program (Doryl B 109-3).

Inasmuch as neither the newly prepared test samples nor the original test samples showed any indication of failure when the thermal shock test was repeated, it is evident that surface stresses sufficient to cause failure were being created by the cleaning or evaporation operations to which these test samples were not subjected. It was felt that the solvent cleaning step would have slight effect on the polymer, even though maximum resin cure is not obtained in this application. Likewise, while the energy of glow discharge cleaning could affect the polymer structure it is more probable that the major effects would result from the heat and vacuum processing with respect to the free diphenyl oxide constituent of the resin. Diphenyl oxide has a boiling point of 288°C. It would therefore be most probable, under the influence of heat and prolonged exposure to high vacuum, i.e. 2×10^{-6} torr, for a protracted period of time, that this component of the present resin system would volatilize, resulting in a volumetric shrinkage of the resin system. The attendant surface stresses could thus increase to the point wherein subsequent stressing from thermal cycling would be sufficient to cause failure. Some solvent leaching of the diphenyl oxide could also be expected during cleaning. As a solution to the unstability noted a Novalac type of diphenyl oxide was suggested for further study which precludes free diphenyl oxide residue in the resin.

4.1.8 Appendices

4.1.8.1 Appendix I - Resistance

Measurements for Thermal Cycling Test

Key:	Substrate	Permutation* (Part/Substrate-Pod)
	01	GG/A-Au
	02	GG/A-Cu
	03	GG/A-Al(Au)
	04	SS/G-Au
	05	GS/A-Au
	06	GS/A-Cu
	07	GS/A-Al(Au)
	08	GS/G-Au
	09	SS/A-Au
	10	SS/A-Cu
	11	SS/A-Al(Au)
	12	GG/G-Au
	13	SS/G-Cu
	14	GS/G-Cu
	15	GG/G-Cu

*G is Corning 0211 glass

S is silicon

A is Alsimag 614 alumina, American Lava Corp., Chattanooga, Tenn.

RESISTANCE OF INTERCONNECTION PAIR IN OHMS

Substrate	Initial	25 Cycles	50 Cycles	75 Cycles	100 Cycles
01	.506	1.490	1.800	1.500	1.480
	.190	.300	.337	.361	.747
	.401	.720	.744	.762	.795
	.227	.281	.279	.290	.327
	.313	.955	----	----	----
	.507	1.294	1.280	1.253	1.287
	.436	1.094	1.197	1.252	1.290
	.238	.594	.650	.670	.690
	.141	.338	1.290	1.450	1.600
02	.115	.134	.150	.157	.152
	.103	.124	.133	.140	.138
	.119	.136	.146	.150	.156
	.166	.281	.367	.912	.798
	.134	.241	.338	.352	.389
	.080	.155	.141	.221	.194
	.114	.149	.167	.222	.257
	.092	.176	.212	.304	.374
03	.256	.316	.337	.333	.372
	.216	.233	.244	.250	.261
	.229	.271	.303	.315	.314
	.165	.159	.180	.191	.173
	.320	.360	.377	.381	.408
	.365	.573	.632	.656	.710
	.250	.311	.337	.353	.362
	.304	1.695	2.000	2.350	2.902
04	.601	.760	.870	.912	.963
	.497	2.260	2.770	5.000	6.000
	.458	4.770	4.770	----	----
	.560	1.540	----	----	----
	.537	----	----	----	----
	.574	1.265	1.630	2.224	2.690
	.580	----	----	----	----
	.616	.887	1.540	1.204	1.542
	.554	.951	1.470	1.627	4.000
	.415	1.361	2.750	4.800	2.330
	.522	----	----	----	----
	.428	8.000	8.000	5.207	5.700
	.352	1.221	1.400	1.800	2.990
	.421	10.000	10.000	----	----
	.467	----	----	----	----
	.391	.450	.450	----	4.700
	.456	2.200	2.200	----	3.060

Substrate	Initial	25 Cycles	50 Cycles	75 Cycles	100 Cycles
05	.572	2.231	2.520	3.050	3.360
	.605	2.500	2.500	3.000	3.800
	.631	1.811	3.200	3.500	4.300
	.610	2.800	2.800	2.000	3.600
	.380	4.800	4.800	5.000	8.700
	.552	2.131	4.600	3.100	3.700
	.581	6.260	6.260	5.900	4.700
	.400	2.100	2.100	5.000	6.600
	.630	2.970	5.600	6.900	7.100
06	.558	1.607	1.740	1.910	2.020
	.581	.823	.924	1.000	1.160
	.531	2.650	2.650	5.000	4.200
	.491	4.753	2.200	3.000	----
	.546	.880	.880	1.900	2.800
	.370	.443	.533	.630	.713
	.514	----	----	----	----
	.558	8.000	8.000	9.000	12.000
07	.244	.267	.280	.280	.298
	.383	1.377	2.599	7.281	1.500
	.205	.378	.500	.610	1.200
	.274	.406	3.300	4.000	3.100
	.178	.197	.190	.190	.188
	.318	.371	.394	.418	.430
	.201	1.700	1.700	1.560	1.900
	.416	2.700	2.700	3.000	2.900
08	.273	.291	.300	.311	.319
	.323	.332	.335	.344	.234
	.246	.257	.262	.260	.258
	.334	.339	.340	.342	.342
	.414	.260	1.000	1.049	1.149
	.311	.670	.730	.797	.857
	.321	.333	.340	.343	.345
	.260	.506	.550	.596	.633
	.364	.876	1.135	1.366	1.723
	.307	.859	1.063	1.400	2.820
	.240	1.749	1.660	1.989	6.000
	.354	1.500	1.500	2.019	2.091
	.390	1.060	1.823	2.190	2.770
	.260	2.100	2.100	2.890	4.500
	.380	2.000	2.000	.593	5.990
	.156	.250	.277	.290	.325
	.127	1.620	1.677	2.300	2.900
09	.610	1.230	1.580	2.500	3.160
	.517	1.500	1.420	1.600	2.400
	.614	1.232	2.030	2.300	1.762
	.574	1.742	2.580	3.100	4.180

Substrate	Initial	25 Cycles	50 Cycles	75 Cycles	100 Cycles
09	.587	1.522	4.600	7.800	9.500
	.557	1.280	1.551	2.460	2.500
	.340	.394	1.061	1.090	.425
	.631	.982	1.140	1.280	1.500
	.440	5.000	5.000	5.000	5.000
10	.241	.314	1.800	.365	.689
	.367	1.394	1.900	2.865	2.622
	.262	.904	1.590	1.165	2.960
	.140	.154	.170	.216	.210
	.156	.304	.385	.426	.476
	.383	2.130	1.305	4.100	2.100
	.392	.677	.857	1.000	1.109
	.136	.420	.622	.715	.840
11	.347	1.127	1.712	2.035	2.481
	.393	.960	1.025	1.050	.758
	.407	.810	.905	.950	.978
	.427	.470	.488	.490	.495
	.483	.869	.940	----	----
	.308	.430	.446	----	----
	.274	.333	.395	.474	.559
	.290	.436	.319	.553	.748
12	.312	----	----	----	----
	.300	6.400	6.400	----	----
	.176	1.288	2.100	2.550	3.700
	.190	2.500	2.500	3.800	3.190
	.250	4.500	4.500	5.000	3.890
	.311	1.683	2.400	6.000	8.000
	.291	7.400	7.400	8.000	9.100
	.390	2.180	2.180	2.900	8.900
	.202	.813	.892	1.223	1.650
	.448	----	----	----	----
	.180	1.115	.932	.690	1.520
	.253	3.200	2.500	2.990	2.660
	.583	4.300	6.100	8.300	7.230
	.183	.734	1.117	1.900	5.870
	.223	1.613	.800	2.000	1.690
	.551	1.740	2.200	1.600	2.100
	.381	.600	6.000	3.203	6.300
13	.447	2.684	3.000	3.600	4.990
	.136	1.024	1.472	1.820	3.190
	.264	.894	1.856	2.120	2.220
	.447	2.700	2.720	2.950	3.889
	.401	2.707	----	----	----
	.252	----	----	----	----
	.264	.467	.540	.590	.680
	.525	2.100	2.640	4.600	----

Substrate	Initial	25 Cycles	50 Cycles	75 Cycles	100 Cycles
14	.382	.897	----	----	1.940
	.457	.652	1.210	2.700	2.540
	.348	3.460	2.360	5.200	----
	.244	1.190	1.481	1.680	1.900
	.336	----	----	----	----
	.376	4.100	2.150	3.700	4.640
	.210	.458	2.000	----	----
	.241	2.570	3.000	4.000	3.880
15	.452	.910	1.290	2.480	----
	.396	.555	.618	.645	.717
	.430	.604	2.100	.753	.868
	.488	.947	2.200	1.723	1.478
	.492	7.000	5.000	----	----
	.200	----	----	----	----
	.478	2.937	4.900	4.000	6.850
	.333	1.177	1.400	1.513	2.060

Test Lead Resistance Included in all Measurements = .031

Appendix II - Resistance

Measurements for Low Temperature Storage Test

(Resistance of Interconnection Pairs shown in ohms)

(Test Lead Resistance Included in all measurements = .031)

Key: Parts/Substrate - Pad

where G is Corning 0211 Glass
S is silicon
A is Alsimag 614 alumina, American Lava Corp., Chattanooga, Tenn.

		Initial	Final
GS/A-Au	1	.352	.386
	2	.592	.628
	3	.517	.570
	4	.473	.409
	5	.437	.432
	6	.515	.569
	7	.361	.379
	8	.386	.399
	9	.506	.540
GS/A-Cu	1	.302	.327
	2	.487	.517
	3	.311	.330
	4	.297	.337
	5	.317	.339
	6	.563	.590
	7	.537	.600
	8	.595	.740
GS/A-Al(Au)			
	1	.250	.367
	2	.274	.287
	3	.389	.397
	4	.222	.700
	5	.277	.290
	6	.385	.430
	7	.271	.281
	8	.189	.205

		Initial	Final
SS/A-Au	1	.609	.730
	2	.412	.540
	3	.455	.460
	4	.519	.393
	5	.514	1.200
	6	.530	.470
	7	.597	.514
	8	.454	.467
	9	.474	.497
SG/A-Cu	1	.515	.566
	2	.592	.614
	3	.375	.406
	4	.433	.514
	5	.606	.630
	6	.555	.607
	7	.520	.544
	8	.413	.457
SS/A-Al(Au)			
	1	.434	.449
	2	.611	.649
	3	.485	.511
	4	.422	.434
	5	.436	.447
	6	.551	.570
	7	.497	.522
	8	.554	.622
GG/A-Au	1	.422	.429
	2	.374	.466
	3	.433	.459
	4	.514	.553
	5	.370	.379
	6	.307	.319
	7	.397	.439
	8	.386	.400
	9	.306	.320
GG/A-Al (Au)			
	1	.503	.510
	2	.433	.370
	3	.429	.440
	4	.426	.430
	5	.320	.340
	6	.306	.296
	7	.372	.366
	8	.305	.296

		Initial	Final
GG/A-Cu	1	.598	.685
	2	.544	1.200
	3	.555	.615
	4	.519	.540
	5	.622	.750
	6	.541	.376
	7	.550	.546
	8	.550	.996
GS/G-Au	1	.599	.620
	2	.399	.410
	3	.325	.344
	4	.302	.319
	5	.292	.341
	6	.250	.260
	7	.383	.420
	8	.317	.330
	9	.563	.640
GS/G-Cu	1	.205	.220
	2	.406	.410
	3	.227	.246
	4	.262	.367
	5	.378	.384
	6	.365	.379
	7	.305	.320
	8	.327	.346
GS/G-Al(Au)			
	1	.298	.319
	2	.237	.240
	3	.240	.256
	4	.174	.210
	5	.165	.180
	6	.294	.303
	7	.431	----
	8	.336	.343
SS/G-Au	1	.539	.553
	2	.518	.639
	3	.318	.340
	4	.625	.643
	5	----	----
	6	.272	.323
	7	.536	1.573
	8	.505	.673
	9	.168	.185
	10	.396	.430

		Initial	Final
SS/G-Cu	1	.556	.388
	2	.325	.344
	3	.424	.444
	4	.416	.438
	5	.589	.595
	6	.457	.482
	7	.361	.376
	8	.351	.372
SS/G-Al(Au)			
	1	.507	.542
	2	.385	.449
	3	.388	.329
	4	.289	2.500
	5	.286	.310
	6	.394	.999
	7	----	----
	8	.288	.410
	9	.342	.387
GG/G-Au	1	.557	.570
	2	.625	.752
	3	.486	.504
	4	.342	.359
	5	.472	.489
	6	.403	.576
	7	.516	.549
	8	.365	.389
	9	.602	.736
GG/G-Cu	1	.381	.399
	2	.487	.506
	3	.585	.593
	4	.552	.591
	5	.453	.256
	6	.364	.370
	7	.281	.300
	8	.563	.580
GG/G-Al(Au)			
	1	.551	.564
	2	.515	.460
	3	.263	.282
	4	.252	.273
	5	.401	.482
	6	.251	.290
	7	.360	.390
	8	.404	.429

5.0 OVERALL CONCLUSIONS

5.1 EFFECT OF FILLERS

The use of fillers to change the thermal expansion of both the organic and inorganic materials as a technique for obtaining a thermal match was found effective. Within the schedule alloted, only in the case of the organic was a composition found sufficiently promising for use in experimental models. Given more time for development, it is not unreasonable to expect that an inorganic composition could also have been developed as well.

5.2 CHEMICAL STABILITY

Although the experimental models did not meet the thermal shock or low temperature tests further investigations disclosed this unpredicted behavior as due to a condition of chemical unstability which was not evident until the organic was subjected to temperature for unusually long periods of time in a vacuum. The preliminary test samples attested to the stability that may be expected under more reasonable processing.

5.3 TEMPERATURE CAPABILITY

Although no formal tests were conducted to determine the temperature capability, from the final curing temperature of 200°C it is reasonable to assume that a projected capability of 200°C is within sight of the Doryl.

Using the same argument for the inorganics, with a curing temperature around 450°C, a much higher capability should be a forgone conclusion. The devitrified inorganic is rather unique in that the phase transformation raises its melting point by several hundred degrees to approximately 700°C.

5.4 SUBSTRATE COMPATIBILITY

Although far less cracking was found for the glass substrates, so that at first glance one would conclude that this was a more compatible system, a failure mechanism study disclosed that the glass substrates were actually protected by an interface failure which occurred between the glass and resin.

In conclusion, therefore, it would be erroneous to state one substrate as being more compatible.

5.5 OXIDATION OF FILMS

Aluminum and copper films were found subject to oxidation effects as result of exposure to elevated temperatures in air. A gold flash was found to improve oxidation resistance.

5.6 MOISTURE RESISTANCE

All ten samples undergoing moisture resistance testing showed excellent leakage resistance although three did not meet the test objective of ten megohms at the conclusion of the test. No failures were catastrophic. Examination of the test samples under 30X after the test revealed a limited amount of corrosion. The protective coating used, Silastic 140, was considered adequate.

5.7 SCREENABILITY

The screenability of the inorganics were far superior to the organic. The thermal flow characteristic during curing of the inorganics added measurably to the aesthetic appearance that was obtained. The devitrified product, however, has a somewhat matted texture, so that the vitrified type (glossy) was rated highest on the basis of surface texture.

5.8 THERMAL SHOCK

The thermal shock test with the square chip proved to be the most stringent test of all. The low temperature test, in a sense, may be interpreted as a half cycle thermal shock test since the evidence seems to indicate that failure was due to the cycle rather than the storage.

5.9 RESULTS OF LOW TEMPERATURE AND THERMAL CYCLE

The deposited interconnections in the low temperature storage test failed to meet the resistance stability objective set forth in the technical requirement of a maximum charge of ten percent from initial value after 1000 hours storage. The thermally cycled samples also failed. In addition, the thermally cycled samples developed a number of catastrophic failures. The resistance changes associated with thermal cycling were much larger than the changes as a result of low temperature storage. The mechanism responsible for the catastrophic or large changes in the thermally cycled interconnections in probability also caused the lesser changes in the low temperature storage samples. In reality the low temperature storage may be looked upon as a half cycle of thermal cycling. The difficulties with the thermally cycled interconnections probably stemmed from a combination of shrinkage and lack of plastic deformation in the bridging material, which is the result of the particular combination of processing variables used in fabricating the models for environmental testing.

The resistance change data was plotted separately for each permutation of chip and substrate in order to reveal any pecularities associated with the behavior of a particular permutation. It can be seen that no such special relationship exists, with the possible exception of the glass chips in aluminum substrates, which appear to be exceptionally stable in thermal cycling. Little significance is attached to this result because the variations in processing from one substrate to the next can more than cover this range of resistance behavior. For example, the surface texture of the bridging material applied by screening varied widely but become more controlled as fabrication of the models progressed. The

environmental testing included samples from both early and later stages of model fabrication, so this represents a variable which can affect the results of the environmental testing in an unknown manner. To define the environmental testing more equitably, models should be used which are more representative of the same level of process refinement.

6. RECOMMENDATIONS

As indicated in the analytical section of this report, the investigations demonstrated the difficulty of developing a satisfactory universal bridging material suitable for the wide range of materials and parts geometry specified in Technical Requirement SCL-7638B.

Results indicate the desirability of selecting chip, substrate and bridging material with compatible thermal expansion characteristics.

The combination having the greatest use potential, such as silicon chips on an appropriate substrate should be pursued.

6.1 CHIP

This could be done, for example, by restricting chip material to silicon since this has the greatest potential. There would be no objection to glass chips if thin glass sheet were available that would match silicon in thermal expansion. Actually thin film components can be fabricated directly on the substrate.

Further work should be directed toward developing a technique for mounting square silicon chips on a substrate and interconnecting them. The chips should be square since this is both a more severe test of the bridging material, and a more practical specific application.

6.2 SUBSTRATE

Along the same lines, the substrate should be selected with a match to silicon. Alumina, although meeting the strength requirements, is a poor thermal match for silicon. The choice of substrate material should be left open, with requirements for mechanical strength, electrical isolation, and suitability for use in a flat pack structure being prime considerations. Experiments have shown it can be more practical to mount parts on the substrate surface instead of recessing them flush with the surface. This approach causes a limitation on the resolution of the deposited conductor, but the advantage in eliminating substrate machining is considerable. It is

not anticipated that any new screening problems would arise from having the chip stick out above the substrate surface.

6.3 BRIDGING MATERIAL

Further development of inorganic bridging material with fillers controlling thermal expansion appears promising as indicated by other in-house research. Thermal shock tests have been met using filled inorganics with nominal changes in the resistance of the interconnect. Research to eliminate the occurrence of sharp irregularities of the bridging material is indicated.

6.4 THIN FILM PROCESSING

From the viewpoint of reliability and optimum electrical properties, the sequence of film depositions should be done without exposure to atmosphere.

A distinct advantage would be to have films stable to 500°C in order to be compatible with I.C. fabrication techniques.

6.5 INTERCONNECT RESISTANCES

Interconnect resistances should be designed to be compatible with high sheet resistivity films. The actual maximum permissible resistance is determined by the specific circuit application, but some design freedom can be obtained by proper choice of which part of the overall circuit is contained on each chip. It is desirable to connect between high impedance points. Sheet resistivities of 0.1 to 1 ohm per square are reasonable design values for conductors of three to ten thousand Angstroms thickness depending on the metal, and the surface it is deposited onto.

6.6 ENVIRONMENTAL TESTS

It is suggested that a more critical test to evaluate these materials would be to use active devices. As a time saver, we have found that leads are not required because the pads of the devices can be probed to

obtain curve tracer data. Our own preliminary information indicates this latter test is a more critical criterion.

7. KEY PERSONNEL

In Table 7-1 are listed the key technical personnel and approximate man-hours performed by each.

Table 7-1
Key Personnel

Name	Specialty	Man-Hours
M. Lauriente	Project Manager	502
J. M. Winter	Project Engineer	722
W. A. Ernst	Materials and Processes Manager	8
C. A. Harper	Materials and Processes Engineer	87
C. W. Wyble	Materials and Processes Engineer	307
	Total	1637

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Unclassified
Security Classification

DOCUMENT CONTROL DATA - R&D

(Security classification of title, body of abstract and indexing annotation must be entered when the overall report is classified)

1. ORIGINATING ACTIVITY (Corporate author) Westinghouse Electric Corporation Friendship International Airport Box 746, Baltimore, Maryland	2a. REPORT SECURITY CLASSIFICATION Unclassified 2b. GROUP

3. REPORT TITLE

Planar Integration of Thin Film Units

4. DESCRIPTIVE NOTES (Type of report and inclusive dates)

Final Report, 15 January 1964 to 14 January 1965

5. AUTHOR(S) (Last name, first name, initial)

Lauriente, Michael C. A. Harper
Winter, John M. C. W. Wyble

6. REPORT DATE	7a. TOTAL NO OF PAGES	7b. NO OF REFS
14 January 1965	92	20

8a. CONTRACT OR GRANT NO.	9a. ORIGINATOR'S REPORT NUMBER(S)
Contr No. DA36-039 AMC-03732(E) b. PROJECT NO. 1P6-22001-A-057 (3A99-15-005) c. d.	9b. OTHER REPORT NO(S) (Any other numbers that may be assigned this report)

10. AVAILABILITY/LIMITATION NOTICES

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11. SUPPLEMENTARY NOTES	12. SPONSORING MILITARY ACTIVITY
	U.S. Army Electronics Command U. S. Army Electronics Laboratories Fort Monmouth, New Jersey

13. ABSTRACT

Three organic materials and five inorganic materials were investigated for mounting "chip" parts and silicon semiconductor integrated circuits into recesses in microcircuit wafers of glass and alumina and for their ability to provide a suitable surface for the subsequent formation of a deposited electrical conductor.

On the basis of preliminary thermal cycling tests a lithium silicate filled diphenyl oxide varnish was selected as the most feasible material for the intended application. Deposited electrical conductors were chromium-copper-gold.

Samples were exposed to low temperature, moisture cycling, and thermal shock and evaluated for adhesion of deposited conductors, corrosion and migration, interconnection resistance and insulation resistance.

Test results are given and analyzed and a failure mechanism study conducted to determine origin of failures.

Factual data includes a stress analysis of the assembly system, properties of the various materials investigated, techniques employed for substrate and component fabrication, thin film deposition techniques and flow diagrams of the process employed.

DD FORM 1 JAN 64 1473

Unclassified
Security Classification